1 **INPUT/OUTPUT DATA PROCESSING**
2 .Input/Output expansion
3 .Input/Output addressing
4 ..Address data transfer
5 .Input/Output command process
6 ..Operation scheduling
7 ..Concurrently performing Input/Output operation and other operation unrelated to Input/Output
8 .Peripheral configuration
9 ..Address assignment
10 ..Configuration initialization
11 ..Protocol selection
12 ..As input or output
13 ..By detachable memory
14 ..Mode selection
15 .Peripheral monitoring
16 ..Characteristic discrimination
17 ..Availability monitoring
18 ..Activity monitoring
19 ..Status updating
20 .Concurrent Input/Output processing and data transfer
21 ..Concurrent data transferring
22 .Direct Memory Accessing (DMA)
23 ..Programmed control memory accessing
24 ..By command chaining
25 ..Timing
26 ..Using addressing
27 ..Via separate bus
28 ..With access regulating
29 .Flow controlling
30 .Frame forming
31 .Transfer direction selection
32 .Transfer termination
33 .Data transfer specifying
34 ..Transferred data counting
35 ..Burst data transfer
36 .Input/Output access regulation
37 ..Access dedication
38 ..Path selection
39 ..Access request queuing
40 ..Access prioritization
41 ...Dynamic
42 ...Group
43 ...Physical position
44 ...Prioritized polling
45 ...Time-slot accessing
46 ..Input/Output polling
47 ...Polled interrupt
48 ..Input/Output interrupting
49 ...Masking
50 ...Vectored
51 ..Accessing via a multiplexer
52 .Input/Output data buffering
53 ..Alternately filling or emptying buffers
54 ..Queue content modification
55 ..Contents validation
56 ..Buffer space allocation or deallocation
57 ..Fullness indication
58 .Input/Output process timing
59 ..Processing suspension
60 ..Transfer rate regulation
61 ..Synchronous data transfer
62 .Peripheral adapting
63 ..Universal
64 ..Via common units and peripheral-specific units
65 ..Input/Output data modification
66 ...Width conversion
67 ...Keystroke interpretation
68 ...Data compression and expansion
69 ...Analog-to-digital or digital-to-analog
70 ...Digital-to-digital
71 ...Serial-to-parallel or parallel-to-serial
72 ..Application-specific peripheral adapting
73 ...For user input device
74 ...For data storage device
100 **INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)**
300 .Bus expansion or extension
301 ..Card insertion
302 ...Hot insertion
303 ..Docking station
304 ...Hot docking
104 .System configuring
105 .Protocol
106 ..Using transmitter and receiver
107 .Bus access regulation
108 ..Bus locking
109 ..Bus polling
110 ..Bus master/slave controlling
111 ..Rotational prioritizing (i.e., round robin)
112 ..Bus request queuing
113 ..Centralized bus arbitration
114 ...Static bus prioritization

115 ....Physical position bus prioritization
116 ...Dynamic bus prioritization
117 ...Time-slotted bus accessing
118 ...Delay reduction
119 ..Decentralized bus arbitration
120 ...Hierarchical or multilevel accessing
121 ...Static bus prioritization
122 ....Physical position bus prioritization
123 ...Dynamic bus prioritization
124 ...Time-slotted bus accessing
125 ...Delay reduction
305 .Bus interface architecture
306 ..Bus bridge
307 ...Variable or multiple bus width
308 ...Direct memory access (e.g., DMA)
309 ...Arbitration
310 ...Buffer or que control
311 ...Intelligent bridge
312 ...Multiple bridges
313 ...Peripheral bus coupling (e.g., PCI, USB, ISA, and etc.)
314 ...Common protocol (e.g., PCI to PCI)
315 ...Different protocol (e.g., PCI to ISA)
316 ..Path selecting switch
317 ...Crossbar
200 **ACCESS LOCKING**
220 **ACCESS POLLING**
240 **ACCESS ARBITRATING**
241 .Centralized arbitrating
242 .Decentralized arbitrating
243 .Hierarchical or multilevel arbitrating
244 .Access prioritizing
260 **INTERRUPT PROCESSING**
261 .Multimode interrupt processing
262 .Interrupt inhibiting or masking
263 .Interrupt queuing
264 .Interrupt prioritizing
265 ..Variable
266 .Programmable interrupt processing
267 .Processor status
268 .Source or destination identifier
269 .Handling vector

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**