CLASS 711, ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

SECTION I - CLASS DEFINITION

This class provides, within an electrical computer or digital data processing system, for the following subject matter:

A. Processes and apparatus for addressing memory wherein the processes and apparatus involve significant address manipulating (e.g., combining, translating, or mapping and other techniques for formatting and modifying address data) and are combined with specific memory configurations or memory systems;

B. Processes and apparatus for accessing and controlling memory (e.g., transferring and modifying address data, selecting storage devices, scheduling access); and

C. Processes and apparatus for forming memory addresses (e.g., virtual memory addressing, address translating, translation-lookaside buffers (TLBs), boundary checking, and page mode).

SCOPE OF THE CLASS

(1) Note. In the instance where a peripheral is a memory, classification herein is proper.

(2) Note. Classification herein requires more than nominal recitation of addressing techniques or of memory accessing or controlling in combination with digital data processing systems or data processing. A nominal combination refers to a combination wherein one or more of the means or steps thereof are recited so broadly, and without details, as to constitute a mere identification rather than a description of each means or step.

(3) Note. Memory devices, per se, are classified in their respective device classes. More specifically, registers and data bearing records (e.g., smart cards) are classified elsewhere. Static memory devices including internal elements of memories are classified elsewhere. Display memory organizations and structures (i.e., selective visual display systems) such as memories defined by graphics processing systems and graphics processing that involves interfacing with memory are classified elsewhere. Devices (e.g., printers) that include memory for processing data for static presentation (i.e., for viewing on a fixed medium such as paper) are classified elsewhere. Dynamic magnetic information storage or retrieval devices (e.g., magnetic disks, tapes, drums, etc.) are classified elsewhere. Dynamic information storage or retrieval devices (e.g., optical disks, CD-ROMs, jukebox mechanics, and other storage devices having magnetic and mechanical components) are classified elsewhere. See the SEARCH CLASS notes below.

(4) Note. Processes and apparatus for transferring data between memories of different computers directly (i.e., with minimum or no intervention from main processors of the computers) are classified elsewhere. See the SEARCH CLASS notes below.

(5) Note. Processes and apparatus for direct memory access (DMA) (i.e., the transferring of data between peripherals and memories of a computer or digital data processing system with minimal or no intervention from the main processor of the computer or digital data processing system) are classified elsewhere. See the SEARCH CLASS notes below.

(6) Note. Processes and apparatus for accessing and retrieving instruction data of a fixed or variable length from a memory or buffer and for shifting such instruction data to align it with a physical memory or buffer boundary are classified elsewhere. See the SEARCH CLASS notes below.

SECTION II - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

235, Registers, various subclasses for basic machines and associated indicating mechanisms for ascertaining the number of movements of various devices and machines; machines made from these basic machines alone (e.g., cash registers, voting machines) and in combination with various perfecting features such as printers and recording means; and

various systems controlled by data bearing records (e.g., smart cards).

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), subclass 202 for repeating geometric arrangement of individual structural elements of solid-state devices, and subclasses 368 and 390 for matrix or array of field effect transistors (FETs).

326, Electronic Digital Logic Circuitry, subclasses 37+ for multifunctional or programmable logic (e.g., gate arrays) and subclasses 52+ and 104+ for generic logic functions such as EXOR, AND, OR, NOT and decoding in general.

340, Communications: Electrical, subclasses 1.1 through 16.1 for controlling one or more devices to obtain a plurality of results by transmission of a designated one of plural distinctive control signals over a smaller number of communication lines or channels, particularly subclasses 2.1-2.8 for path selection, subclass 2.81 for tree or cascade selective communication, subclasses 3.1-3.9 for communication systems where status of a controlled device is communicated, subclasses 4.1-4.14 for synchronizing selective communication systems, subclasses 9.1-9.17 for selective communication addressing, subclasses 12.1-12.55 for pulse responsive actuation, and subclasses 14.1-14.69 for selective decoder matrix.

341, Coded Data Generation or Conversion, various subclasses for electrical pulse and digit code converters (e.g., systems for originating or emitting a coded set of discrete signals or translating one code into another code wherein the meaning of the data remains the same but formats may differ).

345, Computer Graphics Processing and Selective Visual Display Systems, subclasses 1.1 through 3.4 for visual display systems with selective electrical control including display memory organization and structure for storing image data and manipulating image data between a display memory and display peripheral, subclasses 530-574 for memory organization and structure for storing images to be displayed, and subclass 521 for graphic processing that involves interfacing with memory.

353, Optics: Image Projectors, subclasses 25+ for selective data retrieval of stored information viewed by a projection means.

358, Facsimile and Static Presentation Processing, subclasses 1.16 and 1.17 for process and apparatus (e.g., printer) that includes memory for processing data for static presentation (i.e., for viewing on a fixed medium such as paper).

360, Dynamic Magnetic Information Storage or Retrieval, (which is an integral part of Class 369 following subclass 18), for record carriers and systems wherein data are stored and retrieved by interaction with a medium and there is relative motion between a medium and a transducer (e.g., magnetic disk drives, tapes, and drums and control thereof, per se), particularly subclasses 72.1+ for locating a specific area in storage.

361, Electricity: Electrical Systems and Devices, subclasses 679.31 through 679.39 for computer storage component combined with housing or mounting arrangement having no data processing or calculating procedures.

365, Static Information Storage and Retrieval, various subclasses for static memory devices including internal elements of the memory, particularly subclass 189.011 for read/write circuits and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements; subclass 189.05 for buffering or latching data being read from or written to memory; subclass 189.08 for logic devices in combination with memory systems; subclasses 200 and 201 for testing of memory systems; and subclass 230.08 for buffering and latching address data being employed to access memory.

369, Dynamic Information Storage or Retrieval, various subclasses for record carriers and systems wherein data are stored and retrieved by interaction with a medium and there is relative motion between a medium and a transducer (e.g., optical disks, CD-ROMs, jukeboxes), particularly subclasses 30.01 through 41.01, 69, and 176-271 for designating or selecting storage media to be used for storage and retrieval.

370, Multiplex Communications, appropriate subclasses for multiplex switching techniques similar to addressing and the handling of memory information signals and for the simultaneous transmission of two or more signals over a common medium, particularly 351 for time division multiplex (TDM) switching, subclass 395.7 for an ATM network with detail of storage access and control, subclasses 475+ for asynchronous TDM communications including addressing, and subclasses 498+ for time division bus transmission.

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 64+ for shift registers.

701, Data Processing: Vehicles, Navigation, and Relative Location, appropriate subclasses for applications of computers in vehicular and navigational environments.

700, Data Processing: Generic Control Systems or Specific Applications, appropriate subclasses and particularly subclasses 1 through 89 for data processing generic control systems and subclasses 90-306 for computer and data processing system applications.

702, Data Processing: Measuring, Calibrating, or Testing, subclass 80 for specified memory location generation for storage of an electrical signal parameter measurement.

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/Decompression, subclasses 1+ for applications of computers in linguistics, subclasses 200+ for applications of computers in speech signal processing, and subclasses 500 through 504 for applications of computers in audio compression/decompression.

705, Data Processing: Financial, Business Practice, Management, or Cost/Price Determination, appropriate subclasses for applications of computers and calculators in business and management environments.

706, Data Processing: Artificial Intelligence, appropriate subclasses for artificial intelligence, per se.

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 781 through 789 for access control to a database or file in a computer environment; subclasses 790 through 812 for database design including data structures and data structure management; subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structures.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 1+ for electric hybrid computers; subclasses 100+ for electric digital calculating computers; and subclasses 800+ for electric analog computers.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural or Processor Synchronization, appropriate subclasses for multiple computer data transfer, particularly subclass 212 for computer-to-computer direct memory accessing and subclasses 213-216 for multicomputer data transfer via shared memory.

710, Electrical Computers And Digital Data Processing Systems: Input/Output, subclasses 1+ for transferring data from one or more peripherals to one or more computers for the latter to process, store, or further transfer or for transferring data from the computers to the peripherals, particularly subclasses 22+ for direct memory access (DMA) (i.e., the transferring of data between peripherals and memories of a computer or digital data processing system with minimal or no intervention from the main processor of the computer or digital data processing system).

712, Electrical Computers And Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 1+ for processing architectures such as MIMD, vector, or array processors; subclass 204 for instruction alignment; subclasses 205+ for instruction fetching;and subclasses 200 through 248 for various instruction processing not involving I/O such as executing.

713, Electrical Computers and Digital Processing Systems: Support, subclass 150 and 181 for multiple computer communication using cryptography; and subclasses 187 and 188 for software program protection or computer virus detection in combination with data encryption.

714, Error Detection/Correction and Fault Detection/Recovery, various subclasses for detecting or correcting errors in generic electrical pulse or pulse coded data and for detecting and recovering from faults of computers, digital data processing systems, and logic level based systems, particularly subclass 702 for memory access (e.g., address permutation); subclasses 710+ for replacement with spare memory components or portion thereof; subclasses 718+ for memory testing; and subclasses 763+ for memory access with error correction, error pointer, or error checking.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

901, Robots, appropriate cross-reference art collections for reprogrammable, multifunction manipulators designed to move devices.

SECTION III - GLOSSARY

The terms below have been defined for purposes of classification in this class and are shown in underlined type when used in the class and subclass definitions. When these terms are not underlined in the definitions, the meaning is not restricted to the glossary definitions below.

ADDRESS DATA

Data that specify a location in a memory.

BUS

A conductor used for transferring data, signals, or power.

COMPUTER

A machine that inputs data, processes data, stores data, and outputs data.

DATA

Representation of information in a coded manner suitable for communication, interpretation, or processing. See ADDRESS DATA, INSTRUCTION DATA, STATUS DATA, and USER DATA in this glossary,

DATA PROCESSING

See PROCESSING below.

DIGITAL DATA PROCESSING SYSTEM

An arrangement of processor(s) in combination with either memory or peripherals, or both, performing data processing.

INFORMATION

Meaning that a human being assigns to data by means of the conventions applied to that data.

INSTRUCTION DATA

Data that represent an operation and identify its operands, if any.

MEMORY

A functional unit to which data can be stored and from which data can be retrieved.

PERIPHERAL

A functional unit that transmits data to or receives data from a computer to which it is coupled (e.g., modems, keyboards, monitors, touch tablet, printers, joy stick, disk and tape drives, etc.).

PROCESSING

Methods or apparatus performing systematic operations upon data or information exemplified by functions such as data or information transferring, merging, sorting, and calculating (i.e., arithmetic operations or logical operations).

Note: In an effort to avoid redundant constructions, in this class, where appropriate, the term address data processing is used in place of address data data processing.

PROCESSOR

A functional unit that interprets and executes instruction data.

STATUS DATA

Data that represent conditions of data, computers, peripherals, memory, etc.

USER DATA

Data other than address data, instruction data, or status data.

SUBCLASSES

1 ADDRESSING COMBINED WITH SPECIFIC MEMORY CONFIGURATION OR SYSTEM:

This subclass is indented under the class definition. Subject matter comprising means or steps for determining one or more values (i.e., address data) that specify one or more locations in a storage medium wherein the means or steps are claimed in combination with a particular configuration or system for storing data.

(1) Note. Classification herein requires significant address manipulating (i.e., more than nominal recitation of an addressing technique). Significant address manipulating is exemplified by address dataprocessing functions such as combining,

translating, mapping, and other techniques associated with forming or modifying address data.

(2) Note. Means or steps for determining a value that specifies a memory location (i.e., address data) must include more than nominal recitation of processing functions and memory components for classification herein.

(3) Note. This subclass and those indented below provide for combinations of data processing, particular memory systems, and significant address data manipulating. Generalized addressing in a digital data processing system is classified elsewhere in this class. See the SEARCH THIS CLASS, SUBCLASS notes below.

(4) Note. This subclass and those indented below may include means (e.g., processor, controller, etc.) or steps for control of a memory of a digital data processing system in combination with memory accessing (e.g., reading, writing). Memory accessing and control for specific memory compositions, hierarchical memory configurations, and shared memory, however, is classified elsewhere. See the SEARCH THIS CLASS, SUBCLASS notes below.

(5) Note. Means or steps for accessing and controlling plural memory configurations (e.g., data farms, "library" systems) that include significant data processing are classified herein. Control systems for delivering storage media (e.g., delivery of robotics or automated tapes or cartridges, selection and delivery of platters), however, are properly classified elsewhere under automated control or another appropriate subclass in the respective device, robotics, and generic control classes. In instances involving significant data processing and significant details of media delivery systems, classification herein is proper.

SEE OR SEARCH THIS CLASS, SUBCLASS:

3 for cache memory addressing.

101 through 116, for storage accessing and control for various memory compositions (e.g., ROM, RAM, CAM, dynamic, detachable, bubble, etc.) with more than nominal data processing.

117 through 146, for storage accessing and control for hierarchical memory with nominal address forming.

147 through 154, for storage accessing and control for shared memory with nominal address forming.

200+, for generalized address forming in data processing systems.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 105+ for digital logic decoding circuits in general.

340, Communications: Electrical, subclasses 14.1 through 14.69 for selective matrix which may be used for control or as a switching means.

345, Computer Graphics Processing and Selective Visual Display Systems, subclasses 530 through 574 for processing indices to locations (or addresses) of stored data elements in a computer graphic processing system.

365, Static Information Storage and Retrieval, subclasses 189.011 for read/write circuits, and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements of the same type.

369, Dynamic Information Storage or Retrieval, subclasses 30.01 through 41.01, 69, and 176-271, as appropriate, for subject matter related to designation or selection of storage medium to be used for storage and retrieval.

370, Multiplex Communications, appropriate subclasses for multiplex switching techniques similar to addressing or the handling of memoryinformation signals.

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation and Audio Compression/ Decompression, subclasses 2+ for memory control scheme combined with linguistics.

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 781 through 789 for access control to a database or file in a computer environment and subclasses 790 through 812 for database design including data structures and data structure management, subclasses 813 through 820 for garbage collection in database environments and subclasses 821 through 831 for file management, file systems and file directory structures.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 3 through 4 for Input/Out addressing, subclass 9 for address assignment for configuring peripherals, subclasses 22-28 for direct memory accessing (DMA) and subclass 316 for system intra-connecting switching.

901, Robots, appropriate cross-reference art collections for reprogrammable, multifunction manipulators designed to move devices.

2 Addressing extended or expanded memory:

This subclass is indented under subclass 1. Subject matter wherein addresses are determined for memory not normally accessible by a base operating system, computer, or digital data processing system components.

(1) Note. Classification here may include virtual addressing techniques; however, virtual memory addressing art which deals with logical addressing techniques as opposed to addressing for physical enhancements, such as extended and expanded memory, is classified elsewhere in this class.

SEE OR SEARCH THIS CLASS, SUBCLASS:

203+, for virtual addressing, per se.

3 Addressing cache memories:

This subclass is indented under subclass 1. Subject matter wherein addresses are generated for memory nearest a processor in a hierarchical memory arrangement (i.e., a cache memory arrangement).

(1) Note. This subclass accommodates particular addressing techniques for cache memory systems. Cache memory accessing and control (i.e., reading and writing) are classified elsewhere in this class. See the SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

117+, for hierarchical memory arrangement accessing and control, including cache memory in subclasses 118 through 146.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclass 49.1 for internal aspects of associative memory.

4 Dynamic-type storage device (e.g., disk, tape, drum):

This subclass is indented under subclass 1. Subject matter wherein address schemes are particular to a data storage device requiring relative motion between a data holding medium and a recording mechanism such as disk, tape, or drum memory.

SEE OR SEARCH CLASS:

360, Dynamic Magnetic Information Storage or Retrieval, which is an integral part of Class 369, following subclass 18, for record carriers and systems wherein information is stored and retrieved by interaction with a medium and there is relative motion between a medium and a transducer (e.g., magnetic disk drive devices and control thereof, per se). See Class 360, subclass 72.2 for addressing and control of recording mechanism to locate the selected area.

369, Dynamic Information Storage or Retrieval, various subclasses for record carriers and systems wherein information is stored and retrieved by interaction with a medium and there is relative motion between a medium and a transducer. Particularly, see subclasses 30.01 through 41.01 for selective addressing of dynamic storage medium.

5 For multiple memory modules (e.g., banks, interleaved memory):
This subclass is indented under subclass 1. Subject matter wherein logical addresses are determined and mapped (e.g., interleaving) across different physical memory arranged in blocks, banks, partitions, etc.

(1) Note. This subclass includes subject matter directed to static column or static row handling in multiple physical memory module addressing.

SEE OR SEARCH THIS CLASS, SUBCLASS:
127 for interleaved cache.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclasses 230.03 and 230.04 for subject matter including plural banks or blocks and alternating between them.

6 Virtual machine memory addressing:
This subclass is indented under subclass 1. Subject matter wherein addresses are determined in a memory system accommodating addressing requirements for software emulation of a target computer or digital data processing system on a base computer or digital data processing system.

(1) Note. Classification here includes virtual addressing techniques (that is, for example, processing logical to physical (real, absolute) address translation entries. Virtual memory addressing deals with logical addressing techniques. Classificaiton here is proper if there is significant virtual memory processing for systems accomodating emulation of a tarte computer of digital data processin system on a base computer or digital data processing system. Logical addressing for physical enhancements, such as extended and expanded memory, is classified elsewhere in theis class.

SEE OR SEARCH THIS CLASS, SUBCLASS:
202 through 210, for address mapping and virtual addressing, per se.

SEE OR SEARCH CLASS:
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.
718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, subclass 1 for virtual machine task or process management.

100 STORAGE ACCESSING AND CONTROL:
This subclass is indented under the class definition. Subject matter comprising means (e.g., a processor, a controller, etc.) or steps for governing memory in a computer or digital data processing system or the passage (e.g., reading, writing) of data thereto.

(1) Note. The subject matter of this subclass and the subclasses thereunder provides for details of how memory is accessed and controlled. Classification herein requires more than nominal recitation of accessing or controlling memory in the context of digital data processing systems or data processing. Examples of significant memory accessing and control data processing include transferring and modifying memoryaddress data, selecting memory devices or memory locations, and scheduling memory accesses.

(2) Note. Storage devices such as static memory devices, holographic stores, disk drives (and the mechanical control of disk drives, e.g., head positioning, substrate speed, etc.), and optical stores, are classified, per se, in their respective device classes.

(3) Note. Subject matter classified herein may include nominal recitations of address data generation, manipulation, and modification. Combinations of a particular memory construct (e.g., cache) with accessing and control and significant addressing as exemplified by data processing functions such as combining, translating, mapping, and other techniques associated with forming and

modifying addresses, however, are classified in superior subclasses directed to such combinations. See the SEARCH THIS CLASS, SUBCLASS notes below.

(4) Note. Classification herein requires more than nominal recitation of means or steps for controlling memory.

(5) Note. This subclass and the subclasses thereunder also provide for subject matter wherein static or dynamic storage forms part of a digital data processing system.

(6) Note. Subject matter classified herein may include nominal recitations of reliability and availability in combination with memory accessing and control. The species of reliability and availability related to data archiving, backup, and device access limiting and security combined with memory accessing and controlling is classified herein. Other species of reliability and availability combined with memory accessing and controlling are classified elsewhere. See the SEARCH THIS CLASS, SUBCLASS notes below.

(7) Note. Memories known as display memory, display buffers, frame buffers, VRAMs, etc., functioning in combination to store image data for image processing are properly classified elsewhere. Subject matter for interfacing between a graphics processor and a memory is classified elsewhere. See the SEARCH THIS CLASS, SUBCLASS notes and SEARCH CLASS notes below for the information handling subclasses relevant to memories acting on display data.

(8) Note. Means or steps for accessing and controlling plural memory configurations (e.g., data farms, "library" systems, etc.) including significant data processing are classified here. Details of control systems for medium delivery such as robotics or automated tape, cartridge, and platter selection and delivery, however, are properly classified elsewhere under automated control or another appropriate subclass in the respective device, robotics, and generic control classes. In instances where there is significant data processing and significant details of medium delivery systems, classification should be based on the hierarchy of classes and classified here.

(9) Note. This subclass is directed to generic memory accessing and control. Database accessing and retrieval is classified elsewhere. See the SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

161+, for reliability and availability combined with memory accessing and control provided for in this array. See the (6) Note for subclass 100 above.

SEE OR SEARCH CLASS:

340, Communications: Electrical, subclasses 1.1 through 16.1 for controlling one or more devices to obtain a plurality of results by transmission of a designated one of plural distinctive control signals over a smaller number of communication lines or channels, particularly subclasses 2.1-2.8 for path selection, subclass 2.81 for tree or cascade selective communication, subclasses 3.1-3.9 for communication systems where status of a controlled device is communicated, subclasses 4.1-4.14 for synchronizing selective communication systems, subclasses 9.1-9.17 for selective communication addressing, subclasses 12.1-12.55 for pulse responsive actuation, and subclasses 14.1-14.69 for selective decoder matrix.

345, Computer Graphics Processing and Selective Visual Display Systems, subclasses 530 through 574 for memory organization and structure for storing images to be displayed and subclasses 531-574 for interfacing between a graphics processor and a memory.

353, Optics: Image Projectors, subclasses 25+ for selective data retrieval of stored information viewed by a projection means.

358, Facsimile and Static Presentation Processing, subclasses 1.16 and 1.17 for static presentation processing combined with memory.

361, Electricity: Electrical Systems and Devices, subclasses 679.31 through 679.39 for computer storage component combined with housing or mounting arrangement having no data processing or calculating procedures.

369, Dynamic Information Storage or Retrieval, subclasses 30.01 through 41.01, 69, and 176-271, as appropriate, for subject matter related to designation or selection of storage medium to be used for storage and retrieval.

370, Multiplex Communications, for the simultaneous transmission of two or more signals over a common medium, particularly subclasses 351+ for time division multiplex (TDM) switching, subclasses 475+ for asynchronous TDM communications including addressing, and subclasses 498+ for time division bus transmission.

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/ Decompression, subclasses 2+ for memory control scheme combined with linguistics.

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 781 through 789 for access control to a database or file in a computer environment, subclasses 790 through 812 for database design including data structures and data structure management, subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structures.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 1+ for combinations of data transfers performed by a peripheral (e.g., I/O processors, DMA, I/O controllers, I/O adapters, etc.) between digital data processing systems or computers and peripherals; subclasses 22+ for Direct Memory Access (DMA) or direct data transfers to or from memory or to or from other peripherals and for data transfers performed by a peripheral between external components such as disk drives, peripheral devices, etc., which involves I/O processing; and subclasses 100+ for connections within a single computer or digital data processing system arrangement such as interfacing, bus arbitration, bus expansion.

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 220+ for processing control and instruction processing, per se, which often includes access to registers surrounding functional units of a processor.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 1+ for reliability and availability combined with memory accessing and control not provided for herein (see the (6) Note above).

717, Data Processing: Software Development, Installation, and Management, subclasses 151 through 161 for software/program optimization of memory usage or other resource usage (e.g., optimization by removing redundancy, eliminating unnecessary memory accesses, etc.).

901, Robots, appropriate cross-reference art collections for reprogrammable, multifunction manipulators designed to move devices.

101 Specific memory composition:

This subclass is indented under subclass 100. Subject matter wherein control of the memory or the accessing thereof is adapted to the type of memory being accessed.

(1) Note. Structures and particulars of the memory device itself are classified in the relevant device class.

(2) Note. Subject matter included herein is directed to the specifics of accessing technique employed to access and control the memory by computers, digital data processing systems, processors, or other users.

(3) Note. The nature of data stored in a memory (i.e., the information) does not make the memory "specific" within the context of this and its indented subclasses (e.g., video or image data, printer buffer, control datamemory, etc.).

(4) Note. Accessing and controlling of a multiport memory, per se, are classified elsewhere in this class. See the SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

131 for multiport cache.

149 for shared multiport memory.

SEE OR SEARCH CLASS:

235, Registers, subclasses 375+ for systems controlled by data bearing records.

313, Electric Lamp and Discharge Devices, subclasses 391+ for cathode ray tube storage devices.

326, Electronic Digital Logic Circuitry, subclasses 37+ for multifunctional or programmable logic (e.g., gate arrays) and subclasses 52+ and 104+ for generic logic functions such as EXOR, AND, OR, NOT, and decoding.

369, Dynamic Information Storage or Retrieval, subclasses 30.01 through 41.01, 69, and 176-271, as appropriate, for subject matter related to designation or selection of storage medium to be used for storage and retrieval.

439, Electrical Connectors, subclasses 43+ for plug board connections and pins, and subclasses 55+ for preformed panel circuit arrangements (e.g., ICs, chips, wafers, etc.).

902, Electronic Funds Transfer, cross-reference art collections 25+ for smart card memories.

102 Solid-state read only memory (ROM):
This subclass is indented under subclass 101. Subject matter including means or steps for accessing solid-state randomly accessible nonvolatile memory (e.g., ROM).

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, appropriate subclasses for storage having a particular internal cell structure (e.g., subclass 94 for read only (i.e., semipermanent) systems), subclasses 189.011 for memory read/write circuits, and subclasses 230.01+ for addressing circuits.

103 Programmable read only memory (PROM, EEPROM, etc.):
This subclass is indented under subclass 102. Subject matter including means or steps for accessing and controlling programmable solid-state nonvolatile memory (e.g., PROM, EPROM, EEPROM, flash, etc.).

104 Solid-state random access memory (RAM):
This subclass is indented under subclass 101. Subject matter including apparatus or method for accessing volatile randomly accessible memory.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 129+ for various memory elements used in random access memory construction.

105 Dynamic random access memory:
This subclass is indented under subclass 104. Subject matter including means or steps for accessing volatile memory requiring periodic refreshing (e.g., DRAM, Dynamic RAM, etc.).

106 Refresh scheduling:
This subclass is indented under subclass 105. Subject matter including specifics of coordinating refreshing operations with other system operations.

(1) Note. This subclass is proper for subject matter directed to coordinating refresh scheduling with other system events, accesses, requirements, etc., external to the memory cells. However, coordinating the timing requirements within a memory cell or composite thereof is classified elsewhere. See the SEARCH CLASS notes below.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, appropriate subclasses for timing requirements at the cell level and for storage having a particular internal cell structure (e.g., subclass 222 for memory refreshing).

107 Ferrite core:

This subclass is indented under subclass 101. Subject matter comprising arrays of magnetizable rings as the individual storage elements.

(1) Note. In the 1960"s the term "core memory" referred exclusively to memory with ferrite cores. Also at that time, the main memory of large systems were exclusively of this type. As the art progressed, the term core memory became a holdover to refer to the system"s main memory, regardless of the actual type of memory being used. Therefore, if core memory is claimed, the specification should be checked to see if the memory is indeed core memory (i.e., ferrite memory) for classification here; otherwise, it should be treated as solid-state memory and classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:

102+, for ROM accessing and control.

104+, for RAM accessing and control.

108 Content addressable memory (CAM):

This subclass is indented under subclass 101. Subject matter including memory of the type where elements are addressed according to the stored contents (e.g., associative memory, etc.).

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories or content addressable memories (CAM), per se.

109 Shift register memory:

This subclass is indented under subclass 101. Subject matter including memory of the type where elements are arranged to serially pass the stored contents from one location to an adjacent location, or for use in data format conversion within a digital data processing system.

(1) Note. Employing shift registers as part of the system memory for transferring data within a digital data processing system is classified here; however, the specifics of the interconnections and control of shift register memories is classified elsewhere. See the SEARCH CLASS notes below.

(2) Note. Although data format conversion may form part of the overall combination in this subclass, data format conversion, per se, is classified elsewhere. See the SEARCH CLASS notes below.

SEE OR SEARCH CLASS:

235, Registers, subclasses 441+, 492, and 493 for electrical records and record sensors (i.e., IC cards).

341, Coded Data Generation or Conversion, appropriate subclasses for digital to digital code converting.

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 64+ for shift registers and subclasses 107+ and 118+ for counters.

110 Circulating memory:

This subclass is indented under subclass 109. Subject matter wherein the contents of a register may be passed in a recirculating fashion among a group of adjacent registers (e.g., ring buffers, barrel shifters, etc.).

111 Accessing dynamic storage device:

This subclass is indented under subclass 101. Subject matter including accessing memory of the type where a storage medium is moved relative to a transducer (e.g., magnetic or paper tape, punched cards, etc.).

(1) Note. This and indented subclasses provide for dynamic storage combined with significant digital data processing system elements and functions.

SEE OR SEARCH CLASS:

235, Registers, subclasses 375+ for various systems controlled by data bearing records, subclasses 419+ for record controlled calculators, and subclasses 435+ for coded record sensors.

360, Dynamic Magnetic Information Storage or Retrieval, subclasses 72.1+ for locating a specific area in storage.

369, Dynamic Information Storage or Retrieval, various subclasses for the arrangement of information within dynamic storage alone.

112 Direct access storage device (DASD):

This subclass is indented under subclass 111. Subject matter wherein devices employing a medium capable of being accessed directly and by so doing skipping past portions of the medium.

(1) Note. For purposes of this definition, memory devices known typically as disks, drums, etc., are considered to be of the direct access type whereas tapes are not.

113 Caching:

This subclass is indented under subclass 112. Subject matter wherein the DASD is used as a dedicated hierarchically intermediate store or with a dedicated hierarchically intermediate store.

(1) Note. Caching in this subclass is (a) being performed by a DASD device or (b) being supplied by another device in combination with a DASD. Caching, per se, is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:

117+, for hierarchical memory accessing and control and caching, per se.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories and caches under their class definition.

114 Arrayed (e.g., RAIDs):

This subclass is indented under subclass 112. Subject matter where a plurality of direct access devices are arranged in an array and files or portions thereof are stored on more than one of the direct access storage devices.

(1) Note. This subclass is appropriate for redundant arrays of inexpensive disks (RAID).

(2) Note. See the (6) Note to subclass 100 for systems directed to reliability and availability of DASDs. See the SEARCH CLASS notes below.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 39+ for programmable gate arrays.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 20+ for systems directed to parallel data transfer.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 5.1 through 6.32 for systems directed to reliability and availability of DASDs.

115 Detachable memory:

This subclass is indented under subclass 101. Subject matter wherein the memory is of the solid-state type and can be readily physically connected and disconnected manually, without the aid of any tools, for temporary or transient purposes (e.g., replaceable memory cartridges, smart cards, etc.).

SEE OR SEARCH THIS CLASS, SUBCLASS:

2 for addressing extended/expanded memory.

SEE OR SEARCH CLASS:

235, Registers, subclasses 441+, 492, and 493 for electrical records and record sensors (i.e., IC cards).

463, Amusement Devices: Games, subclass 44 for a cartridge for game memory storage.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclass 300 for bus expanding/extending and hot card inserting.

116 Bubble memory:

This subclass is indented under subclass 101. Subject matter wherein the memory is of the solid-state type comprising one or more series

of persistent microscopically small magnetized bubbles on a thin film substrate.

117 Hierarchical memories:
This subclass is indented under subclass 100. Subject matter wherein the memory being accessed or controlled is in an arrangement consisting of more than one ordered level of memory.

118 Caching:
This subclass is indented under subclass 117. Subject matter wherein portions of the data stored in slower main memory are transferred to faster memory between processor(s) and the main memory.

SEE OR SEARCH THIS CLASS, SUBCLASS:
113 for systems where a cache memory is created within a DASD or dedicated to a DASD device.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories and caches at the cell level.

119 Multiple caches:
This subclass is indented under subclass 118. Subject matter employing plural cache memories arranged between at least one processor and at least one main memory.

120 Parallel caches:
This subclass is indented under subclass 119. Subject matter further comprising means or steps for employing plural cache memories arranged at the same ordinal level between at least one processor and at least one main memory.

121 Private caches:
This subclass is indented under subclass 119. Subject matter further comprising means or steps for employing plural cache memories where at least one of the caches is exclusively associated with a respective one of a plurality of processors.

122 Hierarchical caches:
This subclass is indented under subclass 119. Subject matter further comprising means or steps for caching at a plurality of different hierarchical levels (e.g., main cache coupled to an on-chip cache).

123 User data cache and instruction data cache:
This subclass is indented under subclass 119. Subject matter further comprising means or steps for employing separate or partitioned cache(s) for separately storing portions of instruction data and user data, respectively.

(1) Note. This physical separation of instruction data and user data is often referred to as Harvard architecture in the art and associated literature.

124 Cross-interrogating:
This subclass is indented under subclass 119. Subject matter wherein an individual cache system must announce to other cache systems or check with other cache systems which may possibly contain a copy of a given cached location prior to or upon modification or appropriation of data at a given cached location.

125 Instruction data cache:
This subclass is indented under subclass 118. Subject matter further comprising means or steps using a single cache dedicated to caching instruction data.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 200 through 219, 220+ and 300 for instructional data processing, particularly 216+ for instruction dependency checking and resolution.

126 User data cache:
This subclass is indented under subclass 118. Subject further comprising means or steps for using a single cache dedicated to caching user data.

127 Interleaved:
This subclass is indented under subclass 118. Subject matter wherein consecutive cache memory locations are located in different memory components.

SEE OR SEARCH THIS CLASS, SUBCLASS:
5 for interleaving in combination with multiple memory modules with significant addressing.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclasses 230.03 and 230.04 for subject matter including plural banks or blocks and alternating between them.

128 Associative:
This subclass is indented under subclass 118. Subject matter further comprising organizing a cache system where any block in main memory can be mapped to any block in the cache (fully associative) or where the cache is divided into sets of blocks and individual blocks of main memory are mapped to any of the blocks of a particular corresponding set (that is, for example, set associative).

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories or content addressable memories (CAM), per se.

129 Partitioned cache:
This subclass is indented under subclass 118. Subject matter further comprising means or steps for dividing the cache into independent sections or domains.

130 Shared cache:
This subclass is indented under subclass 118. Subject matter further comprising means or steps for providing caching functions to a plurality of processors from single cache.

131 Multiport cache:
This subclass is indented under subclass 118. Subject matter further comprising caches composed of multiport memory thereby allowing simultaneous reads from the cache by plural processors.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclass 230.05 for multiple port access devices.

132 Stack cache:
This subclass is indented under subclass 118. Subject matter further comprising means or steps for caching stack data.

133 Entry replacement strategy:
This subclass is indented under subclass 118. Subject matter including provisions for determining when the contents of a cache location may be replaced with other data.

SEE OR SEARCH THIS CLASS, SUBCLASS:
203+, for various generalized virtual addressing teachings.

134 Combined replacement modes:
This subclass is indented under subclass 133. Subject matter using a combination that includes more than one entry replacement determination mode.

135 Cache flushing:
This subclass is indented under subclass 133. Subject matter including provisions to clear or reset the cache or associated flags.

136 Least recently used:
This subclass is indented under subclass 133. Subject matter where the determination is made based upon the time since the last access to the contents of a given location.

137 Look-ahead:
This subclass is indented under subclass 118. Subject matter where selected data from main memory are retrieved into the cache prior to any request from the processor for the selected data.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Archi-

tectures and Instruction Processing (e.g., Processors), subclass 205 for fetching, 207 for prefetching, and 233+ for branch prediction.

138 Cache bypassing:
This subclass is indented under subclass 118. Subject matter wherein selected memory accesses are not placed into or retrieved from the cache.

139 No-cache flags:
This subclass is indented under subclass 138. Subject matter including provisions for marking selected locations of main memory so that the contents are not cached.

140 Cache pipelining:
This subclass is indented under subclass 118. Subject matter wherein one access sequence to the cache memory is started before a prior access sequence is completed.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 205+.

141 Coherency:
This subclass is indented under subclass 118. Subject matter further comprising means or steps not specifically covered above for assuring that the data stored in the cache memory and those of the main memory are either identical or controlled so that stale and current data are not confused with each other.

(1) Note. The subject matter in this subclass is also called cache consistency or cache currency in the art.

SEE OR SEARCH THIS CLASS, SUBCLASS:
161+, for various reliability methods under accessing and control allowed by the (6) Note for subclass 100 above, such as archiving and backup.

SEE OR SEARCH CLASS:
707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases, subclasses 687 through 704 for database integrity in databases, and subclasses 790 through 812 for database design including data structures and data structure management.
714, Error Detection/Correction and Fault Detection/Recovery, subclass 1 for reliability and availability in digital data processing systems, per se, including subclasses 5.1 through 6.32 for memory or peripheral subsystem affected fault recovery.
715, Data Processing: Presentation Processing of Document, Operator Interface Processing, and Screen Saver Display Processing, subclasses 255 through 272 for developing or changing a document wherein one or more elements of document are added, deleted, or modified, or including means or steps for storing the resultant altered document or the alterations.

142 Write-through:
This subclass is indented under subclass 141. Subject matter where, as contents of the cache are changed, the changes are also posted to main memory substantially simultaneously.

143 Write-back:
This subclass is indented under subclass 141. Subject matter where, as contents of the cache are changed, the changes are not posted to main memory immediately, but rather changes to a block are posted upon the occurrence of a predetermined event.

144 Cache status data bit:
This subclass is indented under subclass 141. Subject matter wherein coherency for each unit or block of data includes associated identifier bit(s) to indicate the validity status of an associated cached location.

(1) Note. For this subclass, validity status bits can indicate whether data are modified, valid, dirty, etc.

145 Access control bit:

This subclass is indented under subclass 141. Subject matter wherein each unit or block of memory or cache includes associated identifier bit(s) to indicate ownership of or restricted access to the unit or block.

(1) Note. For this subclass, access control bits can indicate whether the associated cached location is exclusive, shared, read only, locked, etc.

146 Snooping:

This subclass is indented under subclass 141. Subject matter further comprising cache memory monitoring an associated address bus to determine if access to a cached location occurs by another cache memory or other user (e.g., DMA, peripherals, etc.).

SEE OR SEARCH CLASS:

710, Electrical Computers And Digital Data Processing Systems: Input/Output, subclasses 100+ for system interconnecting, particularly subclasses 107+ for bus access regulating.

147 Shared memory area:

This subclass is indented under subclass 100. Subject matter wherein at least a portion of the memory being accessed or controlled is solid-state memory that iscommon to a plurality of users (e.g., a CPU and a DMA controller, multiple CPUs, etc.) or a plurality of tasks (e.g., in a multitasking system) or both.

SEE OR SEARCH THIS CLASS, SUBCLASS:

169, for memory access pipelining.

SEE OR SEARCH CLASS:

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases, subclasses 687 through 704 for data integrity in databases, subclasses 781 through 789 for access control to a database or file in a computer environment, subclasses 790 through 812 for database design including data structures and data structure management, subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structures.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural Processor Synchronization, subclasses 213 through 216 for a plurality of computers transferring data through one or more memories accessible by the plurality of computers.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, subclasses 102 through 108 for process scheduling involving balancing the work load or resources, memory use, register use, resource availability, time constraints, semaphores, and mutual exclusion mechanisms used for programs or process synchronization.

148 Plural shared memories:

This subclass is indented under subclass 147. Subject matter wherein plural independent memories are shared.

149 Multiport memory:

This subclass is indented under subclass 147. Subject matter including means or steps for controlling shared memory capable of supporting a plurality of simultaneous read accesses.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclass 230.05 for multiple port access devices.

150 Simultaneous access regulation:

This subclass is indented under subclass 147. Subject matter including provisions for controlling simultaneous memory access requests.

SEE OR SEARCH CLASS:

710, Electrical Computers And Digital Data Processing Systems: Input/Output, subclasses 36+ for I/O access regulating; subclasses 107+ for access regulating and arbitration within a digital data processing system; subclasses 200 through 244 for generalized locking, polling, access arbitrating; and subclasses 260+ for interrupt processing.

151 Prioritized access regulation:

This subclass is indented under subclass 147. Subject matter including provisions for assigning priority for use in handling simultaneous memory access requests.

SEE OR SEARCH CLASS:

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 36+ for I/O access regulating; subclasses 107+ for access regulating and arbitration within a digital data processing system; and subclasses 200 through 269 for generalized locking, polling, access arbitrating, and interrupt processing.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, subclass 103 for priority scheduling of process (e.g., deciding which resources to use, deciding which jobs to do first and what order to do them; scheduling constraints may include resource characteristics such as performance, availability, data coherency, etc.).

152 Memory access blocking:

This subclass is indented under subclass 147. Subject matter including provisions for selectively restricting access to memory areas.

SEE OR SEARCH CLASS:

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 36+ for I/O access regulating; subclasses 107+ for access regulating and arbitration within a digital data processing system; and subclasses 200 through 244 for generic access locking, access regulating, or access arbitration in data processing system.

153 Shared memory partitioning:

This subclass is indented under subclass 147. Subject matter further comprising means for dividing or segmenting a given logical shared memory area into independent sections or domains.

SEE OR SEARCH CLASS:

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases, subclasses 687 through 704 for data integrity in databases, subclasses 781 through 789 for access control to a database or file in a computer environment, subclasses 790 through 812 for database design including data structures and data structure management, subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structure.

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclass 228 for processing control and instruction processing for context preserving; subclass 229 for processing control and instruction processing for mode switch or change.

717, Data Processing: Software Development, Installation, and Management, appropriate subclasses for significant details of the construction, analysis, or modification of computer languages.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, appropriate subclasses for processing task management, in particular subclass 107 and 108 for multi-tasking and context switching.

719, Electrical Computers and Digital Processing Systems: Interprogram Com-

munication or Interprocess Communication (IPC), appropriate subclasses for interprogram or interprocess communication.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

154 Control technique:
This subclass is indented under subclass 100. Subject matter including particular means or steps for controlling memory accesses not specifically provided for above.

SEE OR SEARCH CLASS:

714, Error Detection/Correction and Fault Detection/Recovery, subclass 702 for memory access, subclasses 710+ for replacement with spare memory component or portion of memory component, subclasses 763+ for memory testing and memory accessing with error correction.

155 Read-modify-write (RMW):
This subclass is indented under subclass 154. Subject matter including provisions for performing an access operation where the contents of a given memory location are read and then overwritten in a single access operation.

156 Status storage:
This subclass is indented under subclass 154. Subject matter including provisions for storing data associated with memory accessing and control.

(1) Note. Examples of status data include control status words, program status words, etc.

157 Interleaving:
This subclass is indented under subclass 154. Subject matter wherein consecutive memory addresses are in nonadjacent physical locations.

SEE OR SEARCH THIS CLASS, SUBCLASS:

5 for interleaving in combination with multiple memory modules with significant addressing.

127 for cache interleaving where consecutive cache memory locations are located in different memory components.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 230.03 and 230.04 for subject matter including plural banks or blocks and alternating between them.

158 Prioritizing:
This subclass is indented under subclass 154. Subject matter including banks or modules which are arranged so that a given physical memory element has access priority over another.

159 Entry replacement strategy:
This subclass is indented under subclass 154. Subject matter including provisions for determining when the data stored in a particular memory location may be replaced.

SEE OR SEARCH THIS CLASS, SUBCLASS:

133+, for cache entry replacement strategies.

160 Least recently used (LRU):
This subclass is indented under subclass 159. Subject matter wherein the determination is made based upon the time since the last access to the contents of a given location.

161 Archiving:
This subclass is indented under subclass 154. Subject matter wherein the control technique prevents the corruption, loss, alteration, or disclosure of data by storing.

SEE OR SEARCH CLASS:

380, Cryptography, appropriate subclasses for cryptographic processing in general.

713, Electrical Computers and Digital Processing Systems: Support, subclasses 150 through 181 for multiple computer communication using cryptography and subclasses 187 and 188 for software program protection or computer virus detection in combination with data encryption.

714, Error Detection/Correction and Fault Detection/Recovery, subclass 1 for diagnostic testing or monitoring of a digital data processing system for reliability purposes comprising power fail-safe functions, fault detection, or anticipation of a failure; more specifically, subclasses 5.1 through 6.32 for memory or peripheral subsystem affected recovery, subclass 42 for memory component fault, and subclass 54 for storage content error detection or notification, subclasses 718-723 for reliability and availability in memory accessing and control such as isolating failed memory and storing redundant data with recitation of the recovery, fault, or failure.

717, Data Processing: Software Development, Installation, and Management, subclasses 168 through 172 for software upgrading or updating and subclasses 174-178 for software installation including local and remote software (e.g., operating system, application program, and other executable program) loading, copying, or installing onto a target storage medium such as a hard disk, tape drive, or other memory device.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

162 Backup:

This subclass is indented under subclass 161. Subject matter wherein a verbatim redundant copy of the data is made.

SEE OR SEARCH THIS CLASS, SUBCLASS:

165 for movement or transfers of data amongst locations within a same memory level.

SEE OR SEARCH CLASS:

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 5.1 through 6.32 and subclasses 718-723 for reliability and availability in memory accessing and control such as isolating failed memory and storing redundant data with recitation of the recovery, fault, or failure.

163 Access limiting:

This subclass is indented under subclass 154. Subject matter wherein memory entry is restricted.

SEE OR SEARCH CLASS:

455, Telecommunications, subclass 26.1 for subject matter which blocks access to a signal source or otherwise limits usage of modulated carrier equipment.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 36+ for access regulating of peripheral to computer or vice versa; subclasses 107+ for regulating access of processors or memories to a bus; and subclasses 200 through 244 for generic access locking, access regulating, or access arbitration in data processing system.

713, Electrical Computers and Digital Processing Systems: Support, subclasses 182 through 186 for system access control based on cryptographic identification, and subclasses 187 and 188 for software program protection or computer virus detection in combination with data encryption.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 763+ for memory access block coding and subclass 805 for storage accessing error/fault detection techniques.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

164 With password or key:

This subclass is indented under subclass 163. Subject matter wherein authorization code information (e.g., password, key other than encryption key, etc.) is required for memory access.

(1) Note. This subclass does not provide for cryptographic keys. See below.

SEE OR SEARCH CLASS:

455, Telecommunications, subclass 26.1 for subject matter which blocks access to a signal source or otherwise limits usage of modulated carrier equipment.

705, Data Processing: Financial, Business Practice, Management, or Cost/Price Determination, subclass 18 for handling security or user identification provision to either prevent unauthorized use or access.

713, Electrical Computers and Digital Processing Systems: Support, subclass 187 and 188 for software program protection or computer virus detection in combination with data encryption.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 763+ for memory access block coding and subclass 805 for storage accessing error/fault detection techniques.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

165 Internal relocation:

This subclass is indented under subclass 154. Subject matter including provisions for moving or copying data from one location in a given memory to another location in the given memory or another memory at the same hierarchical level.

(1) Note. This subclass does not provide for DMA. See below.

SEE OR SEARCH CLASS:

710, Electrical Computers And Digital Data Processing Systems: Input/Output, subclasses 22+ for transferring data via the I/O mechanism of DMA.

166 Resetting:

This subclass is indented under subclass 154. Subject matter including provisions for clearing or initializing the contents of a given memory location.

(1) Note. This subclass provides for setting a portion of memory to an initial condition (e.g., filling all locations with zeros).

SEE OR SEARCH CLASS:

713, Electrical Computers and Digital Processing Systems: Support, subclass 1 for digital data processing system initialization or configuration (e.g., initializing, setup, configuration, or resetting) allocating extended or expanded memory, speci device drivers, paths, files, buffers, disk management, etc.; subclass 2 for loading initialization program (e.g., booting, BIOS, IPL, bootstrap, etc.); and subclass 100 for reconfiguring (e.g., changing system settings) of system settings, per se.

167 Access timing:

This subclass is indented under subclass 100. Subject matter including provisions for controlling or coordinating the sequence of operations that make up a memory access.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 93 through 98 for clocking or synchronizing of logic stages or gates.

370, Multiplex Communications, subclass 507 wherein the clock frequency adjustment of one station is based upon information about status of clock signals originating at other stations of the system.

375, Pulse or Digital Communications, subclasses 354+ for synchronizing the operation of pulse or digital receiving or transmitting mechanisms.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural Processor Synchronization, subclass 248 for multicomputer synchronization in a network.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclass 61 for synchronous data transfer in I/O process timing.

712, Electrical Computers and Digital Processing Systems: Processing Archi-

tectures and Instruction Processing (e.g., Processors), subclasses 245 through 248 for processing sequence control.

713, Electrical Computers and Digital Processing Systems: Support, subclasses 400+ for details relating to the timing control or timing regulation of any one or combination of digital data processing system components according to a periodic sequence of clock/ timing pulses (e.g., synchronous time control, time delay, cycle control, cycle steal, etc.).

714, Error Detection/Correction and Fault Detection/Recovery, subclass 12 for fault recovery synchronization of redundantly operating processors.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, appropriate subclasses for task and process scheduling.

168 Concurrent accessing:

This subclass is indented under subclass 167. Subject matter further including means or steps wherein multiple memory accesses are initiated substantially simultaneously.

SEE OR SEARCH CLASS:

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, subclass 107 and 108 for multitasking and time sharing/slicing.

169 Memory access pipelining:

This subclass is indented under subclass 167. Subject matter further including means or steps wherein a first access to memory is initiated before a second access is completed.

(1) Note. Pipelined instruction data processing is classified elsewhere. See the SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH CLASS:

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 205+ for instruction fetching, subclasses 214+ for instruction issuing, subclasses 233+ for branching instruction processing.

713, Electrical Computers and Digital Processing Systems: Support, subclass 2 for loading initializing program.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, appropriate subclasses for task management and control related to process or job execution.

170 Memory configuring:

This subclass is indented under subclass 100. Subject matter in which the allocation of memory space is specified or the layout is automatically determined.

(1) Note. Configuration at booting via software is classified elsewhere in this class. See the SEARCH THIS CLASS, SUBCLASS notes below.

(2) Note. Assigning operating characteristics to peripherals is classified elsewhere in this class. See the SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH CLASS:

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases; subclasses 687 through 704 for data integrity in databases; subclasses 781 through 789 for access control to a database or file in a computer environment; subclasses 790 through 812 for database design including data structures and data structure management; subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structures.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data

Transferring or Plural Processor Synchronization, subclasses 220 through 222 for network computer configuring.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 8+ for assigning operating characteristics to peripherals or peripheral configuring and subclass 104 for utilizing a hardware structure for providing to a digital data processing system component the arrangement of the digital data processing system including characteristics of the digital data processing system"s components.

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclass 228 for processing control and instruction processing for context preserving, subclass 229 for processing control and instruction processing for mode switch or change.

713, Electrical Computers and Digital Processing Systems: Support, subclasses 1+ for digital data processing system initialization or configuration (e.g., initializing, set up, configuration, or resetting) allocating extended or expanded memory, specifying device driver, path, file, buffer, disk management, etc.; subclass 100 for reconfiguring of system setting, per se.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 3+ for reconfiguring in the event of a fault under fault recovery, reliability, and availability.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, appropriate subclasses for task management, in particular subclass 104 for resource allocation (e.g., deciding how best to use the available resources to get the job done) and also subclasses 107 and 108 for multitasking and context switching.

171 Based on data size:
This subclass is indented under subclass 170. Subject matter comprising means or steps for allocating memory space based on the amount of storage space required.

172 Based on component size:
This subclass is indented under subclass 170. Subject matter comprising means or steps for allocating memory based on the size of each physical solid-state memory.

173 Memory partitioning:
This subclass is indented under subclass 170. Subject matter further comprising means for dividing or segmenting a given logical memory into independent sections or domains.

200 ADDRESS FORMATION:
This subclass is indented under the class definition. Subject matter comprising means or steps for determining or modifying a value which specifies a location in at least one memory.

(1) Note. The subject matter of this subclass and the subclasses thereunder includes, for example, virtual memory addressing, address translation, translation look-aside buffers (TLBs), boundary checking, and page-mode addressing.

(2) Note. The subject matter also includes deriving new address data from existing address data.

(3) Note. The location in memory may include data for forming further an address (e.g., address mapping is classified herein).

(4) Note. Means or steps for addressing or for storing data in one or more memory cells of a storage medium having one or more specific, internal cell elements is classified elsewhere. See the SEARCH CLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

1 for addressing combined with specific memory configurations (e.g., extended/expanded memory, cache memory, dynamic memory, etc.).

3 for cache memory addressing.

101 through 116, for storage accessing and control for various memory compositions (e.g., ROM, RAM, CAM, dynamic, detachable, bubble, etc.) with more than nominal data processing.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 104 through 108 for digital logic decoding circuits in general.

340, Communications: Electrical, subclasses 9.1 through 9.17 for selective communication addressing and subclasses 14.1-14.69 for selective decoder matrix which may be used for control or as a switching means.

345, Computer Graphics Processing and Selective Visual Display Systems, subclasses 530 through 574 for processing indices to locations (or addresses) of stored data elements in a computer graphic processing system.

360, Dynamic Magnetic Information Storage or Retrieval, subclass 72.2 for addressing and control of recording mechanism to locate the selected area.

365, Static Information Storage and Retrieval, subclass 189.011 for read/write circuits and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements of the same type.

369, Dynamic Information Storage or Retrieval, various subclasses for record carriers and systems wherein information is stored and retrieved by interaction with a medium and there is relative motion between a medium and a transducer. Particularly, see subclasses 30.01 through 41.01 for selective addressing of dynamic storage medium.

370, Multiplex Communications, appropriate subclasses for multiplex switching techniques similar to addressing and the handling of memoryinformation signals (e.g., subclasses 351+ for packetized multiplexed communications).

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/Decompression, subclasses 2+ for memory control scheme combined with linguistics.

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases, subclasses 687 through 704 for data integrity in databases, subclasses 781 through 789 for access control to a database or file in a computer environment, subclasses 790 through 812 for database design including data structures and data structure management, subclasses 813 through 820 for garbage collection in database environments, and subclasses 821 through 831 for file management, file systems and file directory structures.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 3 through 4 for Input/Output addressing; subclass 9 for address assignment for configuring peripherals, subclasses 22-28 for direct memory accessing including addressing techniques; and subclass 316 for system intra-connecting switching.

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 208+ for instruction decoding involving start or initial address generation; subclass 230 for generating the address of the next micro-instruction.

201 Slip control, misaligning, boundary alignment:

This subclass is indented under subclass 200. Subject matter wherein the value determination takes into account a memory size constraint.

(1) Note. This subclass will accept range or limit checking, boundary crossing, and related memory boundary issues (e.g., (a) handling a boundary fixed length field to accommodate data size or position and boundary checking and (b) incrementing addresses within a page).

202 Address mapping (e.g., conversion, translation):
This subclass is indented under subclass 200. Subject matter including translating (i.e., converting) processormemoryaddress data to physical memoryaddress data through a mechanism which defines a correspondence between the addresses.

(1) Note. The subject matter in this and the indented subclasses is aimed at determining a physical address using a mapping technique.

(2) Note. Classification here is proper for direct mapping for a segmented memory not being used in a virtual memory system.

203 Virtual addressing:
This subclass is indented under subclass 202. Subject matter wherein the mapping allows an application to view available memory resources as a uniform primary memory.

SEE OR SEARCH THIS CLASS, SUBCLASS:
6 for address mapping for virtual machines.

204 Predicting, look-ahead:
This subclass is indented under subclass 203. Subject matter wherein means or steps are utilized for optimizing address determination by, for example, anticipating a next address or prefetching addresses.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 205+ for instruction fetching, subclass 207 for profetching of instructions and 233+ for branch prediction.

205 Directories and tables (e.g., DLAT, TLB):
This subclass is indented under subclass 204. Subject matter wherein a memory space is employed for registering indexes and the like to real or physical address spaces in a predicting or look-ahead arrangement.

(1) Note. A directory table is a mechanism for storing virtual (i.e., logical) to physical (i.e., real, absolute) address translation entries that are used in combination with methods of predicting or prefetching.

(2) Note. DLAT is a term of art referring to Directory Look-Aside Table; TLB is a term of art referring to Translation Look-Aside Buffer.

206 Translation tables (e.g., segment and page table or map):
This subclass is indented under subclass 203. Subject matter wherein directories (e.g., maps) are employed for converting address data in a first form (e.g., virtual, logical) to address data in a second form (e.g., physical, absolute).

(1) Note. This subclass and its indented subclasses are intended for generalized applications of tables not classifiable in the combinations above.

(2) Note. This area also provides for mechanisms for storing virtual (i.e., logical) to physical (i.e., real, absolute) address translation entries that are of general use in virtual memory.

(3) Note. This subclass will accept table walking which generally requires accesses to main memory.

207 Directory tables (e.g., DLAT, TLB):
This subclass is indented under subclass 206. Subject matter wherein a memory space is employed for registering indexes and the like to real or physical address spaces.

(1) Note. These mechanisms convert address data from a virtual address to a physical address without the need for accessing translation tables in main memory (e.g., utilizing cache for virtual to physical translation).

(2) Note. DLAT is a term of art referring to Directory Look-Aside Table; TLB is a term of art referring to Translation Look-Aside Buffer.

SEE OR SEARCH THIS CLASS, SUBCLASS:
3 for cache memory addressing.

208 Segment or page table descriptor:
This subclass is indented under subclass 206. Subject matter wherein an entry, word, or other data is maintained and is utilized in the translation.

209 Including plural logical address spaces, pages, segments, blocks:
This subclass is indented under subclass 203. Subject matter wherein portions of memory are organized or managed in accordance with a predetermined mapping scheme.

(1) Note. This subclass includes art directed to addressing variable-sized pages, segments, and blocks.

210 Resolving conflict, coherency, or synonym problem:
This subclass is indented under subclass 202. Subject matter including compensating for situations when addresses map to the same location (e.g., synonym problems or alias addresses).

SEE OR SEARCH CLASS:
714, Error Detection/Correction and Fault Detection/Recovery, subclass 180 for reliability and availability in general in digital data processing systems.

211 Address multiplexing or address bus manipulation:
This subclass is indented under subclass 200. Subject matter including address bus modifying, multiplexing addresses, or adapting to various bus widths.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclass 300 for bus extending or expanding and subclasses 305-317 for bus architectures.

212 Varying address bit-length or size:
This subclass is indented under subclass 200. Subject matter wherein bits are added or subtracted from existing address data to generate other address data.

213 Generating prefetch, look-ahead, jump, or predictive address:
This subclass is indented under subclass 200. Subject matter wherein look-ahead, predictive, or jump address data are formed.

(1) Note. Prefetching, look-ahead, etc., for virtual memory addressing are classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
203+, for virtual memory addressing.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 205+ and 207 and 233+ respectively.

214 Operand address generation:
This subclass is indented under subclass 200. Subject matter wherein data relevant to an instruction and used by an instruction are used to form the address.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), subclasses 200 through 219, 220+ and 300 for instruction processing, particularly subclasses 233 through 244 for branching instruction processing.

215 In response to microinstruction:
This subclass is indented under subclass 200. Subject matter wherein microcode is stored in memory and particular addressing mechanisms at the microinstruction level are employed.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Archi-

tectures and Instruction Processing (e.g., Processors), particularly subclasses 200 through 219, 220+ and 300 for instruction processing, particularly 245+ for microsequencing processing; and subclasses 1+ for digital data processing system architecture.

216 Hashing:

This subclass is indented under subclass 200. Subject matter wherein an address value (i.e., key other than an encryption key) is manipulated to form an index value.

(1) Note. This subclass does not provide for cryptographic keys. See below.

SEE OR SEARCH CLASS:

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclass 698 for database integrity using hash, subclasses 705 through 721 for database searching, per se, and subclass 747 for hash in index generation.

713, Electrical Computers and Digital Processing Systems: Support, subclass 187 and 188 for software program protection or computer virus detection in combination with data encryption.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

217 Generating a particular pattern/sequence of addresses:

This subclass is indented under subclass 200. Subject matter wherein values specifying memory locations are determined according to a predetermined algorithm.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 230.03 and 230.04 for subject matter including plural banks or blocks and alternating between them.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 718 through 720 for testing memories utilizing patterns of addresses and data.

218 Sequential addresses generation:

This subclass is indented under subclass 217. Subject matter wherein the pattern created is seriatim.

SEE OR SEARCH CLASS:

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, appropriate subclasses for generic pulse counting circuits and systems.

219 Incrementing, decrementing, or shiftingcircuitry:

This subclass is indented under subclass 200. Subject matter utilizing particular hardware that adds by 1, subtracts by 1, and multiplies or divides by 2n (where n is an integer).

SEE OR SEARCH CLASS:

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, appropriate subclasses for generic pulse counting circuits and systems.

220 Combining two or more values to create address:

This subclass is indented under subclass 200. Subject matter wherein results from the interaction of two or more other data provide the address (e.g., generalized indirect addressing, indexing, prefixing, base + sag/tag + set, bit insertion).

221 Using table:

This subclass is indented under subclass 200. Subject matter having a memory space of general utility for registering indexes and like data related to address generation (e.g., fixed offsets, conditions, or status).

SEE OR SEARCH THIS CLASS, SUBCLASS:

202+, for tables used in mapping or translating.

E-SUBCLASSES

The E-subclasses in U.S. Class 711 provide for methods and apparatus for addressing or allocating computer memory space including space management and address translation. They also provide for methods and means

for protecting against unauthorized use of memory and protection against loss of memory contents.

E12.001 ACCESSING, ADDRESSING, OR ALLOCATING WITHIN MEMORY SYSTEMS OR ARCHITECTURES (EPO):

This main group provides for methods and apparatus for addressing or allocating computer memory space including space management and address translation. It also provides for methods and means for protecting against unauthorized use of memory and protection against loss of memory contents. This subclass is substantially the same in scope as ECLA classification G06F12/00.

E12.002 Addressing or allocation; relocation (EPO):

This subclass is indented under subclass E12.001. This subclass is substantially the same in scope as ECLA classification G06F12/02.

E12.003 With multidimensional access, e.g., row/column, matrix, etc. (EPO):

This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/02B.

E12.004 With look-ahead addressing means (EPO):

This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/02C.

E12.005 User addresses space allocation, e.g., contiguous or noncontiguous base addressing, etc. (EPO):

This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/02D.

E12.006 Free address space management (EPO):

This subclass is indented under subclass E12.005. This subclass is substantially the same in scope as ECLA classification G06F12/02D2.

E12.007 In block-addressed memory (EPO):

This subclass is indented under subclass E12.006. This subclass is substantially the same in scope as ECLA classification G06F12/02D2E.

E12.008 In block-erasable memory, e.g., flash memory etc. (EPO):

This subclass is indented under subclass E12.007. This subclass is substantially the same in scope as ECLA classification G06F12/02D2E2.

E12.009 Garbage collection, i.e., reclamation of unreferenced memory (EPO):

This subclass is indented under subclass E12.006. This subclass is substantially the same in scope as ECLA classification G06F12/02D2G.

E12.01 Using reference counting (EPO):

This subclass is indented under subclass E12.009. This subclass is substantially the same in scope as ECLA classification G06F12/02D2G2.

E12.011 Incremental or concurrent garbage collection, e.g., in real-time systems, etc. (EPO):

This subclass is indented under subclass E12.009. This subclass is substantially the same in scope as ECLA classification G06F12/02D2G4.

E12.012 Generational garbage collection (EPO):

This subclass is indented under subclass E12.011. This subclass is substantially the same in scope as ECLA classification G06F12/02D2G4G.

E12.013 Multiple users address space allocation, e.g., using different base addresses, etc. (EPO):

This subclass is indented under subclass E12.005. This subclass is substantially the same in scope as ECLA classification G06F12/02D4.

E12.014 Using tables or multilevel address translation means (EPO):

This subclass is indented under subclass E12.005. This subclass is substantially the same in scope as ECLA classification G06F12/02D6.

E12.015 Addressing variable-length words or parts of words (EPO):

This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/04.

E12.016 In hierarchically structured memory systems, e.g., virtual memory systems, etc. (EPO):

This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/08.

E12.017 Addressing of memory level in which access to desired data or data block requires associative addressing means, e.g. cache, etc. (EPO):

This subclass is indented under subclass E12.016. This subclass is substantially the same in scope as ECLA classification G06F12/08B.

E12.018 Using pseudo-associative means, e.g., set-associative, hashing, etc. (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B10.

E12.019 For peripheral storage systems, e.g., disc cache, etc. (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B12.

E12.02 With dedicated cache, e.g., instruction or stack, etc. (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B14.

E12.021 Using selective caching, e.g., bypass, partial write, etc. (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B18.

E12.022 Using clearing, invalidating, or resetting means (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B20.

E12.023 Multi-user, multiprocessor, multiprocessing cache systems (EPO):

This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B4.

E12.024 With multilevel cache hierarchies (EPO):

This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4L.

E12.025 With network or matrix configuration (EPO):

This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4N.

E12.026 Cache consistency protocols (EPO):

This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P.

E12.027 Using directory methods (EPO):

This subclass is indented under subclass E12.026. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P2.

E12.028 Copy directories (EPO):

This subclass is indented under subclass E12.027. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P2C.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E12.033, for local copy tags for implementing a bus snooping protocol.

E12.029 Associative directories (EPO):

This subclass is indented under subclass E12.027. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P2A.

E12.03 Distributed directories, e.g., linked lists of caches, etc. (EPO):

This subclass is indented under subclass E12.027. This subclass is substantially the

same in scope as ECLA classification G06F12/08B4P2D.

E12.031 Limited pointers directories; state-only directories without pointers (EPO):
This subclass is indented under subclass E12.027. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P2E.

E12.032 With concurrent directory accessing, i.e., handling multiple concurrent coherency transactions (EPO):
This subclass is indented under subclass E12.027. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P2R.

E12.033 Using a bus scheme, e.g., with bus monitoring or watching means, etc. (EPO):
This subclass is indented under subclass E12.026. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P4.

E12.034 In combination with broadcast means, e.g., for invalidation or updating, etc. (EPO):
This subclass is indented under subclass E12.033. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P4B.

E12.035 For main memory peripheral accesses, e.g., I/O or DMA, etc. (EPO):
This subclass is indented under subclass E12.033. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P4P.

E12.036 With software control, e.g., noncacheable data, etc. (EPO):
This subclass is indented under subclass E12.026. This subclass is substantially the same in scope as ECLA classification G06F12/08B4P6.

E12.037 With cache invalidating means (EPO):
This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4J.

E12.038 With shared cache (EPO):
This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4S.

E12.039 For multiprocessing or multitasking (EPO):
This subclass is indented under subclass E12.023. This subclass is substantially the same in scope as ECLA classification G06F12/08B4T.

E12.04 With main memory updating (EPO):
This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B2.

E12.041 Organization and technology of caches (EPO):
This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B22.

E12.042 Of parts of caches, e.g., directory or tag array, etc. (EPO):
This subclass is indented under subclass E12.041. This subclass is substantially the same in scope as ECLA classification G06F12/08B22D.

E12.043 With plurality of cache hierarchy levels (EPO):
This subclass is indented under subclass E12.041. This subclass is substantially the same in scope as ECLA classification G06F12/08B22L.

E12.044 Multiple simultaneous or quasi-simultaneous cache accessing (EPO):
This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B6.

E12.045 Cache with multiple tag or data arrays being simultaneously accessible (EPO):
This subclass is indented under subclass E12.044. This subclass is substantially the same in scope as ECLA classification G06F12/08B6M.

E12.046 Partitioned cache, e.g., separate instruction and operand caches, etc. (EPO):
This subclass is indented under subclass E12.045. This subclass is substantially the same in scope as ECLA classification G06F12/08B6M2.

E12.047 Cache with interleaved addressing (EPO):
This subclass is indented under subclass E12.045. This subclass is substantially the same in scope as ECLA classification G06F12/08B6M4.

E12.048 Cache with multi-port tag or data arrays (EPO):
This subclass is indented under subclass E12.044. This subclass is substantially the same in scope as ECLA classification G06F12/08B6N.

E12.049 Overlapped cache accessing, e.g., pipeline, etc. (EPO):
This subclass is indented under subclass E12.044. This subclass is substantially the same in scope as ECLA classification G06F12/08B6P.

E12.05 By multiple requestors (EPO):
This subclass is indented under subclass E12.049. This subclass is substantially the same in scope as ECLA classification G06F12/08B6P2.

E12.051 With reload from main memory (EPO):
This subclass is indented under subclass E12.049. This subclass is substantially the same in scope as ECLA classification G06F12/08B6P4.

E12.052 Cache access modes (EPO):
This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B16.

E12.053 Burst mode (EPO):
This subclass is indented under subclass E12.052. This subclass is substantially the same in scope as ECLA classification G06F12/08B16B.

E12.054 Page mode (EPO):
This subclass is indented under subclass E12.052. This subclass is substantially the same in scope as ECLA classification G06F12/08B16D.

E12.055 Parallel mode, e.g., in parallel with main memory or CPU, etc. (EPO):
This subclass is indented under subclass E12.052. This subclass is substantially the same in scope as ECLA classification G06F12/08B16F.

E12.056 Variable-length word access (EPO):
This subclass is indented under subclass E12.052. This subclass is substantially the same in scope as ECLA classification G06F12/08B16V.

E12.057 With pre-fetch (EPO):
This subclass is indented under subclass E12.017. This subclass is substantially the same in scope as ECLA classification G06F12/08B8.

E12.058 Address translation (EPO):
This subclass is indented under subclass E12.016. This subclass is substantially the same in scope as ECLA classification G06F12/10.

E12.059 Using page tables, e.g., page table structures, etc. (EPO):
This subclass is indented under subclass E12.058. This subclass is substantially the same in scope as ECLA classification G06F12/10D.

E12.06 Involving hashing techniques, e.g., inverted page tables, etc. (EPO):
This subclass is indented under subclass E12.059. This subclass is substantially the same in scope as ECLA classification G06F12/10D2.

E12.061 Using associative or pseudo-associative address translation means, e.g., translation look-aside buffer (TLB), address translation buffer (ATB), address cache, etc. (EPO):
This subclass is indented under subclass E12.058. This subclass is substantially the same in scope as ECLA classification G06F12/10L.

E12.062 Associated with data cache (EPO):

This subclass is indented under subclass E12.061. This subclass is substantially the same in scope as ECLA classification G06F12/10L4.

E12.063 Data cache being concurrently physically addressed (EPO):

This subclass is indented under subclass E12.062. This subclass is substantially the same in scope as ECLA classification G06F12/10L4P.

E12.064 Data cache being concurrently virtually addressed (EPO):

This subclass is indented under subclass E12.062. This subclass is substantially the same in scope as ECLA classification G06F12/10L4V.

E12.065 For multiple virtual address spaces, e.g., segmentation, etc. (EPO):

This subclass is indented under subclass E12.061. This subclass is substantially the same in scope as ECLA classification G06F12/10L2.

E12.066 Decentralized address translation, e.g., in distributed shared memory systems, etc. (EPO):

This subclass is indented under subclass E12.058. This subclass is substantially the same in scope as ECLA classification G06F12/10M.

E12.067 For peripheral accesses to main memory, e.g., DMA, etc. (EPO):

This subclass is indented under subclass E12.058. This subclass is substantially the same in scope as ECLA classification G06F12/10P.

E12.068 For multiple virtual address spaces, e.g., segmentation, etc. (EPO):

This subclass is indented under subclass E12.058. This subclass is substantially the same in scope as ECLA classification G06F12/10S.

E12.069 Replacement control (EPO):

This subclass is indented under subclass E12.016. This subclass is substantially the same in scope as ECLA classification G06F12/12.

E12.07 Using replacement algorithm (EPO):

This subclass is indented under subclass E12.069. This subclass is substantially the same in scope as ECLA classification G06F12/12B.

E12.071 Of the least frequently used type, e.g., with individual count value, etc. (EPO):

This subclass is indented under subclass E12.07. This subclass is substantially the same in scope as ECLA classification G06F12/12B2.

E12.072 With age list, e.g., queue, MRU-LRU list, etc. (EPO):

This subclass is indented under subclass E12.07. This subclass is substantially the same in scope as ECLA classification G06F12/12B4.

E12.073 Being minimized, e.g., nonMRU, etc. (EPO):

This subclass is indented under subclass E12.072. This subclass is substantially the same in scope as ECLA classification G06F12/12B4B.

E12.074 Being generated by decoding array or storage (EPO):

This subclass is indented under subclass E12.072. This subclass is substantially the same in scope as ECLA classification G06F12/12B4C.

E12.075 With special data handling, e.g., priority of data or instructions, pinning, errors, etc. (EPO):

This subclass is indented under subclass E12.07. This subclass is substantially the same in scope as ECLA classification G06F12/12B6.

E12.076 Using additional replacement algorithm (EPO):

This subclass is indented under subclass E12.075. This subclass is substantially the same in scope as ECLA classification G06F12/12B6B.

E12.077 Adapted to multidimensional cache systems, e.g., set-associative, multi-cache, multi-set, or multilevel, etc. (EPO):

This subclass is indented under subclass E12.07. This subclass is substantially the same in scope as ECLA classification G06F12/12B8.

E12.078 Addressing physical block of locations, e.g., base addressing, module addressing, memory dedication, etc. (EPO):
This subclass is indented under subclass E12.002. This subclass is substantially the same in scope as ECLA classification G06F12/06.

(1) Note. This group is limited to module addressing or allocation.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E12.005, for base addressing.

E12.079 Interleaved addressing (EPO):
This subclass is indented under subclass E12.078. This subclass is substantially the same in scope as ECLA classification G06F12/06A.

E12.08 Address space extension (EPO):
This subclass is indented under subclass E12.078. This subclass is substantially the same in scope as ECLA classification G06F12/06C.

E12.081 For memory modules (EPO):
This subclass is indented under subclass E12.08. This subclass is substantially the same in scope as ECLA classification G06F12/06C2.

E12.082 For I/O modules, e.g., memory mapped I/O, etc. (EPO):
This subclass is indented under subclass E12.08. This subclass is substantially the same in scope as ECLA classification G06F12/06C4.

E12.083 Combination of memories, e.g., ROM and RAM, etc., to permit replacement or supplementing of words in one module by words in another module (EPO):
This subclass is indented under subclass E12.078. This subclass is substantially the same in scope as ECLA classification G06F12/06D.

E12.084 Configuration or reconfiguration (EPO):
This subclass is indented under subclass E12.078. This subclass is substantially the same in scope as ECLA classification G06F12/06K.

E12.085 With centralized address assignment (EPO):
This subclass is indented under subclass E12.084. This subclass is substantially the same in scope as ECLA classification G06F12/06K2.

E12.086 And decentralized selection (EPO):
This subclass is indented under subclass E12.085. This subclass is substantially the same in scope as ECLA classification G06F12/06K2D.

E12.087 With decentralized address assignment (EPO):
This subclass is indented under subclass E12.084. This subclass is substantially the same in scope as ECLA classification G06F12/06K4.

E12.088 Address being position dependent (EPO):
This subclass is indented under subclass E12.087. This subclass is substantially the same in scope as ECLA classification G06F12/06K4P.

E12.089 With feedback, e.g., presence or absence of unit detected by addressing, overflow detection, etc. (EPO):
This subclass is indented under subclass E12.084. This subclass is substantially the same in scope as ECLA classification G06F12/06K6.

E12.09 Multi-configuration, e.g., local and global addressing, etc. (EPO):
This subclass is indented under subclass E12.084. This subclass is substantially the same in scope as ECLA classification G06F12/06K8.

E12.091 Protection against unauthorized use of memory (EPO):
This subclass is indented under subclass E12.001. This subclass is substantially the same in scope as ECLA classification G06F12/14.

(1) Note. This subclass covers protection against unauthorized access to memory

E12.092 By using cryptography (EPO):
This subclass is indented under subclass E12.091. This subclass is substantially the

same in scope as ECLA classification G06F12/14B.

E12.093 By checking subject access rights (EPO):
This subclass is indented under subclass E12.091. This subclass is substantially the same in scope as ECLA classification G06F12/14D.

E12.094 Key-lock mechanism (EPO):
This subclass is indented under subclass E12.093. This subclass is substantially the same in scope as ECLA classification G06F12/14D1.

E12.095 In virtual system, e.g., with translation means, etc. (EPO):
This subclass is indented under subclass E12.094. This subclass is substantially the same in scope as ECLA classification G06F12/14D1A.

E12.096 Using access table, e.g., matrix or list, etc. (EPO):
This subclass is indented under subclass E12.093. This subclass is substantially the same in scope as ECLA classification G06F12/14D2.

E12.097 In hierarchical protection system, e.g., privilege levels, memory rings, etc. (EPO):
This subclass is indented under subclass E12.093. This subclass is substantially the same in scope as ECLA classification G06F12/14D3.

E12.098 By checking object accessibility, e.g., type of access defined by the memory independently of subject rights, etc. (EPO):
This subclass is indented under subclass E12.091. This subclass is substantially the same in scope as ECLA classification G06F12/14C.

E12.099 Protection being physical, e.g., cell, word, block, etc. (EPO):
This subclass is indented under subclass E12.098. This subclass is substantially the same in scope as ECLA classification G06F12/14C1.

E12.1 For module or part of module (EPO):
This subclass is indented under subclass E12.099. This subclass is substantially the same in scope as ECLA classification G06F12/14C1A.

E12.101 For range (EPO):
This subclass is indented under subclass E12.099. This subclass is substantially the same in scope as ECLA classification G06F12/14C1B.

E12.102 Protection being virtual, e.g., for virtual blocks or segments before translation mechanism, etc. (EPO):
This subclass is indented under subclass E12.098. This subclass is substantially the same in scope as ECLA classification G06F12/14C2.

E12.103 Protection against loss of memory contents (EPO):
This subclass is indented under subclass E12.001. This subclass is substantially the same in scope as ECLA classification G06F12/16.

END