100 **DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING**
1 .Reliability and availability
2 ..Fault recovery
3 ...By masking or reconfiguration
4.1 ....Of network
4.11 .....Backup or standby (e.g., failover, etc.)
4.12 ......Hot swapping (i.e., while network is up)
4.2 .....Isolate or remove failed node without replacement (e.g., bypassing, re-routing, etc.)
4.21 ......Reintegrate node back into network
4.3 .....Repair failed node without replacement (i.e., on-line repair)
4.4 .....Remote repair
4.5 .....Bus network (e.g., PCI, AGP, etc.)
5.1 ....Of peripheral subsystem
5.11 .....Access processor affected (e.g., I/O processor, MMU, or DMA processor, etc.)
6.1 ....Of memory
6.11 .....Within single memory device (e.g., disk, etc.)
6.12 ......Recovery partition
6.13 ......Isolating failed storage location (e.g., sector remapping, etc.)
6.2 .....Plurality of memory devices (e.g., array, etc.)
6.21 ......Array controller
6.22 ....RAID
6.23 ....Mirror (i.e., level 1 RAID)
6.24 ....ECC, parity, or fault code (i.e., level 2+ RAID)
6.3 ......Backup or standby (e.g., failover, etc.)
6.31 ....Remote repair
6.32 ......Replacement of failed memory device
10 ....Of processor
11 .....Concurrent, redundantly operating processors
12 ......Synchronization maintenance of processors
13 .....Prepared backup processor (e.g., initializing cold backup) or updating backup processor (e.g., by checkpoint message)
14 ....Of power supply
15 ...State recovery (i.e., process or data file)
16 ....Forward recovery (e.g., redoing committed action)
17 .....Reexecuting single instruction or bus cycle
18 ....Transmission data record (e.g., for retransmission)
19 ....Undo record
20 ....Plural recovery data sets containing set interrelation data (e.g., time values or log record numbers)
21 ....State validity check
22 ....With power supply status monitoring
23 ...Resetting processor
24 ...Safe shutdown
25 ..Fault locating (i.e., diagnosis or testing)
26 ...Artificial intelligence (e.g., diagnostic expert system)
27 ...Particular access structure
28 ....Substituted emulative component (e.g., emulator microprocessor)
29 .....Memory emulator feature
30 ....Built-in hardware for diagnosing or testing within-system component (e.g., microprocessor test mode circuit, scan path)
31 ....Additional processor for in-system fault locating (e.g., distributed diagnosis program)
32 ...Particular stimulus creation
33 ....Derived from analysis (e.g., of a specification or by stimulation)
34 ....Halt, clock, or interrupt signal (e.g., freezing, hardware breakpoint, single-stepping)
35 ....Substituted or added instruction (e.g., code instrumenting, breakpoint instruction)

36 ....Test sequence at power-up or initialization
37 ...Analysis (e.g., of output, state, or design)
38.1 ....Of computer software faults
38.11 .....Memory dump
38.12 .....Time-out (i.e., of program)
38.13 .....Interrupt (i.e., halt the program)
38.14 .....By remotely
39 ....Monitor recognizes sequence of events (e.g., protocol or logic state analyzer)
40 ...Component dependent technique
41 ....For reliability enhancing component (e.g., testing backup spare, or fault injection)
42 ....Memory or storage device component fault
43 ....Bus, I/O channel, or network path component fault
44 ....Peripheral device component fault
45 ...Output recording (e.g., signature or trace)
46 ...Operator interface for diagnosing or testing
47.1 ..Performance monitoring for fault avoidance
47.2 ...Threshold
47.3 ...Trends (i.e., expectancy)
48 ..Error detection or notification
49 ...State error (i.e., content of instruction, data, or message)
50 ....State out of sequence
51 .....Control flow state sequence monitored (e.g., watchdog processor for control-flow checking)
52 .....Error checking code
53 ....Address error
54 ....Storage content error
55 ...Timing error (e.g., watchdog timer time-out)
56 ....Bus or I/O channel device fault
57 ...Error forwarding and presentation (e.g., operator console, error display)
699 **PULSE OR DATA ERROR HANDLING**
700 .Skew detection correction
701 .Data formatting to improve error detection correction capability
702 ..Memory access (e.g., address permutation)
703 .Testing of error-check system
704 .Error count or rate
705 ..Pseudo-error rate
706 ..Up-down counter
707 ..Synchronization control
708 ..Shutdown or establishing system parameter (e.g., transmission rate)
709 .Data pulse evaluation/bit decision
710 .Replacement of memory spare location, portion, or segment
711 ..Spare row or column
712 .Transmission facility testing
713 ..For channel having repeater
714 ..By tone signal
715 ..Test pattern with comparison
716 ...Loop-back
717 ..Loop or ring configuration
718 .Memory testing
719 ..Read-in with read-out and compare
720 ...Special test pattern (e.g., checkerboard, walking ones)
721 ..Electrical parameter (e.g., threshold voltage)
722 ..Performing arithmetic function on memory contents
723 ..Error mapping or logging
724 .Digital logic testing
725 ..Programmable logic array (PLA) testing
726 ..Scan path testing (e.g., level sensitive scan design (LSSD))
727 ...Boundary scan
728 ...Random pattern generation (includes pseudorandom pattern)
729 ...Plural scan paths
730 ...Addressing
731 ...Clock or synchronization
732 ..Signature analysis
733 ..Built-in testing circuit (BILBO)
734 ..Structural (in-circuit test)
735 ..Device response compared to input pattern

736 ..Device response compared to expected fault-free response
737 ..Device response compared to fault dictionary/truth table
738 ..Including test pattern generator
739 ...Random pattern generation (includes pseudorandom pattern)
740 ...Having analog signal
741 ...Simulation
742 ...Testing specific device
743 ...Addressing
744 ...Clock or synchronization
745 ..Determination of marginal operation limits
746 .Digital data error correction
747 ..Substitution of previous valid data
748 ..Request for retransmission
749 ...Retransmission if no ACK returned
750 ...Feedback to transmitter for comparison
751 ...Including forward error correction capability
752 ..Forward correction by block code
753 ...Double error correcting with single error correcting code
754 ...Error correction during refresh cycle
755 ...Double encoding codes (e.g., product, concatenated)
756 ....Cross-interleave Reed-Solomon code (CIRC)
757 ...Parallel generation of check bits
758 ...Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)
759 ...Look-up table encoding or decoding
760 ...Threshold decoding (e.g., majority logic)
761 ...Random and burst error correction
762 ...Burst error correction
763 ...Memory access
764 ....Error correct and restore
765 ....Error pointer
766 ....Check bits stored in separate area of memory
767 ....Code word for plural n-bit (n>1) storage units (e.g., x4 DRAM's)
768 ....Error correction code for memory address
769 ....Dynamic data storage
770 .....Disk array
771 .....Tape
772 ....Code word parallel access
773 ....Solid state memory
774 ...Adaptive error-correcting capability
775 ...Synchronization
776 ...For packet or frame multiplexed data
777 ...Hamming code
778 ...Nonbinary data (e.g., ternary)
779 ...Variable length data
780 ...Using symbol reliability information (e.g., soft decision)
781 ...Code based on generator polynomial
782 ....Bose-Chaudhuri-Hocquenghem code
783 ....Golay code
784 ....Reed-Solomon code
785 ....Syndrome computed
786 ..Forward error correction by tree code (e.g., convolutional)
787 ...Random and burst errors
788 ...Burst error
789 ...Synchronization
790 ...Puncturing
791 ...Sequential decoder (e.g., Fano or stack algorithm)
792 ...Trellis code
793 ...Syndrome decodable (e.g., self orthogonal)
794 ...Maximum likelihood
795 ...Viterbi decoding
796 ...Branch metric calculation
797 ..Majority decision/voter circuit
798 .Error detection for synchronization control
799 .Error/fault detection technique
800 ..Parity bit
801 ...Parity generator or checker circuit detail
802 ...Even and odd parity
803 ...Parity prediction
804 ...Plural dimension parity check
805 ...Storage accessing (e.g., address parity check)

806 ..Constant-ratio code (m/n)
807 ..Check character
808 ...Modulo-n residue check character
809 ..Code constraint monitored
810 ...Multilevel coding (n>2)
811 ..Forbidden combination or improper condition
812 ...Specified digital signal or pulse count
813 ...Two key-down detector
814 ...Data timing/clocking
815 ...Time delay/interval monitored
816 ...Two-rail logic
817 ...Noise level
818 ...Missing-bit/drop-out detection
819 ..Comparison of data
820 ...Plural parallel devices of channels
821 ....Transmission facility
822 ...Sequential repetition
823 ....True and complement data
824 ...Device output compared to input

E-SUBCLASSES

The following subclasses beginning with the letter E are E-subclasses. Each E-subclass corresponds in scope to a classification in a foreign classification system, for example, the European Classification system (ECLA). The foreign classification equivalent to an E-subclass is identified in the subclass definition. In addition to US documents classified in E-subclasses by US examiners, documents are regularly classified in E-subclasses according to the classification practices of any foreign Offices identified in parentheses at the end of the title. For example, "(EPO)" at the end of a title indicates both European and US patent documents, as classified by the EPO, are regularly added to the subclass. E-subclasses may contain subject matter outside the scope of this class.Consult their definitions, or the documents themselves to clarify or interpret titles.

E11.001 **ERROR DETECTION; ERROR CORRECTION; MONITORING (EPO)**
E11.002 .Error detection other than by redundancy in data representation, operation, or hardware, or by checking the order of processing (EPO)
E11.003 ..By time limit, i.e., time-out (EPO)
E11.004 ..By count or rate limit, e.g., word- or bit count limit, etc. (EPO)
E11.005 ..By other limits, e.g., analog values, etc. (EPO)
E11.006 ..By bit configuration check, e.g., of formats or tags, etc. (EPO)
E11.007 .Error correction, recovery or fault tolerance using at least two different redundancy techniques and at least one technique not involving redundancy (EPO)
E11.008 ..Fault tolerant software (EPO)
E11.009 ..In regular structures, i.e., all of the systems nodes have the same number of connections per node (EPO)
E11.01 ...Interconnection networks, i.e., comprising interconnecting link and switching elements (EPO)
E11.011 ...Fault-tolerant routing (EPO)
E11.012 ...In rings and buses (EPO)
E11.013 ...In n-dimensional structures, e.g., arrays, trees, cubes, etc. (EPO)
E11.014 ...Neural networks (EPO)
E11.015 ..By degradation, i.e., a slow-down occurs but full processing capability is maintained, e.g., discarding a faulty element or unit, etc. (EPO)
E11.016 ..In systems, e.g., multiprocessors, etc. (EPO)
E11.017 .Security measures, i.e., ensuring safe condition in the event of error, e.g., for controlling element (EPO)
E11.018 .Protecting against parasitic influences, e.g., noise, temperatures, etc. (EPO)
E11.019 .Identification, e.g., of a performed repair, of a defined circuit, etc. (EPO)

E11.02 .Reliability or availability analysis (EPO)
E11.021 .Responding to the occurrence of a fault, e.g., fault tolerance, etc. (EPO)
E11.022 ..Error or fault processing without redundancy, i.e., by taking additional measures to deal with the error/fault (EPO)
E11.023 ...Error or fault handling (EPO)
E11.024 ...Error or fault detection or monitoring (EPO)
E11.025 ...Error or fault reporting or logging (EPO)
E11.026 ...Error or fault localization (EPO)
E11.027 ....By collation, i.e., correlating different errors (EPO)
E11.028 ....By identifying the faulty software code (EPO)
E11.029 ...Error or fault analysis (EPO)
E11.03 ..Error detection or correction by redundancy in data representation, e.g., by using checking codes, etc. (EPO)
E11.031 ...Using codes with inherent redundancy, e.g., n-out-of-m codes (EPO)
E11.032 ...Adding special bits or symbols to the coded information, e.g., parity check, casting out 9's or 11's, etc. (EPO)
E11.033 ....Using arithmetic codes i.e., codes which are preserved during operation, e.g., modulo 9 or 11 check, etc. (EPO)
E11.034 ....In memories (EPO)
E11.035 .....In static stores (EPO)
E11.036 ......Integrated on a chip (EPO)
E11.037 ....In cache or content addressable memories (EPO)
E11.038 ....In sector programmable memories, e.g., flash disk, etc. (EPO)
E11.039 ....In multilevel memories (EPO)
E11.04 ......To protect a block of data words, e.g., CRC, checksum, etc. (EPO)
E11.041 ......To protect individual data words written into, or read out of, the addressable memory subsystem of data processing equipment (EPO)
E11.042 ....Codes or arrangements adapted for a specific type of error (EPO)
E11.043 ....Error in accessing a memory location, i.e., addressing error (EPO)
E11.044 ....Error in check bits (EPO)
E11.045 ....Identification of the type of error (EPO)
E11.046 ....Adjacent error, e.g., error in n-bit (n>1) wide storage units, i.e., package error, etc. (EPO)
E11.047 ....Simple parity (EPO)
E11.048 ....Unidirectional errors (EPO)
E11.049 ....Arrangements adapted for a specific error detection or correction feature (EPO)
E11.05 ....Bypassing or disabling error detection or correction (EPO)
E11.051 ....Updating check bits on partial write, i.e., read/modify/write (EPO)
E11.052 ....Correcting systematically all correctable errors, i.e., scrubbing (EPO)
E11.053 ....Using single parity bit (EPO)
E11.054 ..Error detection or correction of the data by redundancy in hardware (EPO)
E11.055 ...Error detection by comparing the output signals of redundant hardware (EPO)
E11.056 ....In static storage, e.g., matrix, registers, etc. (EPO)
E11.057 ....In coding, decoding circuits, e.g. parity circuits (EPO)
E11.058 ....In communications, e.g., transmission, interfaces, etc. (EPO)
E11.059 ....Control processors, e.g., for sensors, actuators, etc. (EPO)
E11.06 ....With exchange of data between units (EPO)
E11.061 ....With data processors, i.e., data processors compare their computations (EPO)

E11.062 ....In storage with relative movement between record carrier and transducer, e.g., tapes, disks, etc. (EPO)
E11.063 ....In systems, i.e. comprising a multiplicity of resources, e.g., cpu with its memory and I/O, etc. (EPO)
E11.064 ....In arithmetic, logic or counter circuits or a combination thereof, e.g., alu, adder, etc. (EPO)
E11.065 ....In I/O devices or adapters therefor (EPO)
E11.066 .....Displays (EPO)
E11.067 ...Timing and synchronization therein (EPO)
E11.068 ....By using fault tolerant clocks (EPO)
E11.069 ...Using passive fault-masking of the redundant circuits, e.g., by quadding or by majority decision circuits, etc. (EPO)
E11.07 ....Synchronization therefor (EPO)
E11.071 ...Using active fault-masking, e.g., by switching out faulty elements or by switching in spare elements, etc. (EPO)
E11.072 ....In systems, e.g., multiprocessors, etc. (EPO)
E11.073 .....In distributed systems (EPO)
E11.074 ......In regular structures (EPO)
E11.075 ....Array of processors, e.g., systolic arrays, etc. (EPO)
E11.076 ....Hypercubes (EPO)
E11.077 ....Trees (EPO)
E11.078 ....In interconnections, e.g., rings, etc. (EPO)
E11.079 .....Bus (EPO)
E11.08 ....Data exchange between units, e.g., for updating backup units, etc. (EPO)
E11.081 ....For control, e.g., actuators, etc. (EPO)
E11.082 ....In arithmetic units (EPO)
E11.083 ....Redundant power supplies (EPO)
E11.084 ....Masking faults in storage systems using spares and/or by reconfiguring (EPO)
E11.085 .....Removing defective units from operation (EPO)
E11.086 ......Bypassing defective units on a serial bus (EPO)
E11.087 .....With address translations and modifications (EPO)
E11.088 ......Handling defects in a Redundant Array of Inexpensive Disks (RAID) by remapping (EPO)
E11.089 .....Managing spare storage units (EPO)
E11.09 ......Hot spares (EPO)
E11.091 .....Via redundancy in hardware accessing the storage components (EPO)
E11.092 ......Using redundant I/O processors, storage control units or array controllers (EPO)
E11.093 ....With serial buses (EPO)
E11.094 ....To file servers (EPO)
E11.095 ......Connection redundancy between storage system components (EPO)
E11.096 ....With serial buses (EPO)
E11.097 ....To file servers (EPO)
E11.098 .....Using the replication of data, e.g., with two or more copies, etc. (EPO)
E11.099 ......Duplex memories, e.g., twin boot ROMs, etc. (EPO)
E11.1 ....Duplexed caches, e.g., cashe paired with non-volatile storage, etc. (EPO)
E11.101 ......Mirroring, i.e., the concept of maintaining data on two or more units in the same state at all times (EPO)
E11.102 ....Resynchronization of failed mirrors (EPO)
E11.103 ....Mirror management, e.g., pairing of units, etc. (EPO)
E11.104 ....Mirroring on the same storage unit (EPO)
E11.105 ....Mirroring on different storage units with a common controller (RAID 1) (EPO)
E11.106 ....Mirroring with multiple controllers (EPO)
E11.107 ....Asynchronous mirroring (EPO)
E11.108 ....Synchronous mirroring (EPO)
E11.109 ......De-clustering of replicated data (EPO)
E11.11 ......Using more than two copies (EPO)

E11.111 ....In Logic Arrays, e.g., programmable or iterative logic arrays, etc. (EPO)
E11.112 ..Error detection or correction of the data by redundancy in operation (EPO)
E11.113 ...Saving, restoring, recovering or retrying (EPO)
E11.114 ....At machine instruction level (EPO)
E11.115 .....Checkpointing the instruction stream (EPO)
E11.116 .....For bus or memory accesses (EPO)
E11.117 ....Of application data (EPO)
E11.118 .....Backing up, restoring or mirroring files or drives (EPO)
E11.119 ......Backing up, i.e., point-in-time backup (EPO)
E11.12 .....Hardware arrangements for backup (EPO)
E11.121 .....Backup Management techniques (EPO)
E11.122 .....Recovery techniques (EPO)
E11.123 .....Selection of contents (EPO)
E11.124 .....Scheduling policy (EPO)
E11.125 .....For networked environments (EPO)
E11.126 .....Nondisruptive backup (EPO)
E11.127 ......Mirroring (EPO)
E11.128 ......Distributed database systems; Replica control (EPO)
E11.129 .....Synchronization between mobile agents and networked agents (EPO)
E11.13 .....Using logs or checkpoints (EPO)
E11.131 .....In transactions (EPO)
E11.132 ....At operating system level (EPO)
E11.133 .....Boot up procedures (EPO)
E11.134 .....Reconfiguring to eliminate the error (EPO)
E11.135 .....During software upgrading (EPO)
E11.136 .....At file system or disk access level (EPO)
E11.137 .....Restarting or rejuvenating (EPO)
E11.138 .....Resetting or repowering (EPO)
E11.139 .....Cleaning up resources (EPO)
E11.14 .....Suspending and resuming a running system (EPO)
E11.141 .....Transmit or communication errors (EPO)
E11.142 ...Error detection (EPO)
E11.143 ....By time redundancy (EPO)
E11.144 .Error avoidance, e.g., error spreading countermeasures, fault avoidance, etc. (EPO)
E11.145 .Detection or location of defective computer hardware by testing during standby operation or during idle time, e.g., start-up testing, etc. (EPO)
E11.146 ..Verification or detection of system hardware configuration (EPO)
E11.147 ..Logging of test results (EPO)
E11.148 ..Test methods (EPO)
E11.149 ...Power-On Test, e.g., POST, etc. (EPO)
E11.15 ....Configuration test (EPO)
E11.151 ...Background testing (EPO)
E11.152 ...Periodic testing (EPO)
E11.153 ...Test trigger logic (EPO)
E11.154 ..Marginal checking (EPO)
E11.155 ..Testing of logic operation, e.g., by logic analyzers, etc. (EPO)
E11.156 ...Using Fault Dictionaries (EPO)
E11.157 ...Using Expert Systems (EPO)
E11.158 ...Using Neural Networks (EPO)
E11.159 ..Functional testing (EPO)
E11.16 ...Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)
E11.161 ....Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)
E11.162 ....Test or error correction or detection circuits (EPO)
E11.163 ....Test of input/output devices or peripheral units (EPO)
E11.164 ....Test of ALU (EPO)
E11.165 ....Test of interrupt circuits (EPO)
E11.166 ....Test of CPU or processors (EPO)
E11.167 ...By simulating additional hardware, e.g., fault simulation, (EPO)
E11.168 ....Emulators (EPO)
E11.169 ...Built-in tests (EPO)

E11.17 ...Tester hardware, i.e., output processing circuits, etc. (EPO)
E11.171 ....Test interface between tester and unit under test (EPO)
E11.172 ....Using a storage for the test inputs, e.g., test-ROM, script files, etc. (EPO)
E11.173 ....Remote test (EPO)
E11.174 ....Using a dedicated service processor for test (EPO)
E11.175 ....With comparison between actual response and known fault-free response, e.g., signature analyzer, etc. (EPO)
E11.176 ....In Multi-processor systems, e.g., one processor becoming the test master, etc. (EPO)
E11.177 ...Generation of test inputs, e.g., test vectors, patterns or sequences, etc. (EPO)
E11.178 .By checking the correct order of processing (EPO)
E11.179 .Monitoring (EPO)
E11.18 ..With visual or acoustical indication of the functioning of the machine (EPO)
E11.181 ...Visualization of programs or trace data (EPO)
E11.182 ...Display for diagnostics, e.g., diagnostic result display, self-test user interface, etc. (EPO)
E11.183 ....Display of waveforms, e.g., of logic analyzers, etc. (EPO)
E11.184 ...Display of status information (EPO)
E11.185 ....By lamps or LED's (EPO)
E11.186 .....For error or online/offline status (EPO)
E11.187 ....Alarm or error message display (EPO)
E11.188 ....Computer systems status display (EPO)
E11.189 ..Recording or statistical evaluation of computer activity, e.g., of down time, of input/output operation, etc. (EPO)
E11.19 ...Of interconnections, e.g., interconnecting networks, etc. (EPO)
E11.191 ...Of parallel or distributed programming (EPO)
E11.192 ...Performance measurement (EPO)
E11.193 ....Workload generation, e.g., scripts, playback etc. (EPO)
E11.194 .....Benchmarking (EPO)
E11.195 ....Time measurement, e.g., response time, etc. (EPO)
E11.196 .....Of active or idle time (EPO)
E11.197 ...Performance evaluation by modeling or statistical analysis (EPO)
E11.198 ...Performance evaluation by simulation (EPO)
E11.199 ....Trace driven simulation (EPO)
E11.2 ...Performance evaluation by tracing or monitoring (EPO)
E11.201 ....For interfaces, buses (EPO)
E11.202 ....For systems (EPO)
E11.203 ....Address tracing (EPO)
E11.204 ....Data logging (EPO)
E11.205 ....Circuit details, i.e., tracer hardware (EPO)
E11.206 ....For I/O devices (EPO)
E11.207 .Preventing errors by testing or debugging software (EPO)
E11.208 ..Software debugging (EPO)
E11.209 ...Compilers or other tools operating on the source text (EPO)
E11.21 ...Debuggers (EPO)
E11.211 ...Error checking code in the program under test (EPO)
E11.212 ...Tracing methods or tools (EPO)
E11.213 ...By using additional hardware (EPO)
E11.214 ....By making modifications to the CPU (EPO)
E11.215 ....By monitoring the bus (EPO)
E11.216 ....By emulating the CPU (EPO)
E11.217 ..User interfaces for testing or debugging software (EPO)
E11.218 ..Methods or tools for writing reliable software and for evaluating software (EPO)
E11.219 ...Methods or tools to render software testable (EPO)
E11.22 ...Software metrics (EPO)

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

DIGITAL LOGIC TESTING (371/22.1)

FOR 100 .Scan path testing (LSSD) (371/22.3)

FOR 101 .Including test pattern generator (371/27)

DIGITAL DATA ERROR CORRECTION (371/30)

FOR 102 .Block code (371/37.1)

FOR 103 ..Memory access (371/40.1)

FOR 104 .Convolutional code (371/43)

FOR 288 **ERROR/FAULT ANTICIPATION (371/4)**

.Replacement with spare device or system (371/8.1)

FOR 289 ..Transmission facility or channel (371.8.2)

FOR 290 ..Memory (371/10.1)

FOR 291 ..Transmission facility (371/11.2)

FOR 292 ..Data processor or computer (371/11.3)

DIAGNOSTIC TESTING (371/15.1)

FOR 293 .Programmable processor testing (371/16.1)

FOR 294 ..Emulator device (371/16.2)

FOR 295 ..Watchdog timer (e.g., time-out) (371/16.3)

FOR 296 ..Processor within diverse (microwave, photocopier) (371/16.4)

FOR 297 ..Error or fault, logging or tracking (371/16.5)

FOR 298 ..Dedicated maintenance subsystem (371/18)

FOR 299 .Testing of external device by programmable digital computer (371/20)

FOR 300 **ERROR DETECTION FOR SYNCHRONIZATION CONTROL (371/47.1)**

DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING (714/100)

.Reliability and availability (714/1)

..Fault recovery (714/2)

...By masking or reconfiguration (714/3)

FOR 306 ....Of network (714/4)

FOR 307 ....Of memory or peripheral subsystem (714/5)

FOR 308 .....Redundant stored data accessed (e.g., duplicated data, error correction coded data, or other parity-type data) (714/6)

FOR 309 ......Reconfiguration (e.g., adding a replacement storage component (714/7)

FOR 310 .....Isolating failed storage location (e.g., sector remapping) (714/8)

FOR 311 .....Access processor affected (e.g., I/O processor, MMU, DMA processor (714/9)

..Fault locating (i.e., diagnosis or testing) (714/25)

...Analysis (e.g., of output, state, or design) (714/37)

FOR 312 ....Of computer software (714/38)

FOR 313 ..Performance monitoring for fault avoidance (714/47)