CLASS 716, COMPUTER-AIDED DESIGN AND ANALYSIS OF CIRCUITS AND SEMICONDUCTOR MASKS

SECTION I - CLASS DEFINITION

GENERAL STATEMENT OF THE CLASS SUBJECT MATTER

This class provides for computer-based tools, i.e., electrical data processing apparatus and corresponding methods for the following subject matter:

A. Processes or apparatus for sketching, designing, and analyzing circuits or circuit components.

B. Processes or apparatus for planning, designing, analyzing, and devising a template used for creating a mask on a semiconductor wafer.

SCOPE OF THE CLASS

(1)　Note. Processes and apparatus for the use of digital components in various types of digital logic circuitries or active electrical nonlinear circuits or devices are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(2)　Note. Processes and apparatus for connections of electrical components on a printed circuit board are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(3)　Note. Processes and apparatus for computer-controlled semiconductor fabrication are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(4)　Note. Significantly claimed apparatus external to this class, claimed in combination with apparatus under the class definition, which perform data processing circuit design and analysis, are classified in the class appropriate to the external device unless specifically excluded therefrom.

(5)　Note. Nominally claimed apparatus external to this class in combination with apparatus under the class definition is classified in this class unless provided for in the appropriate external class.

SECTION II - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

204,　Chemistry: Electrical and Wave Energy, subclasses 298.01 through 298.39 for coating, forming, or etching apparatus using atomic particles.

250,　Radiant Energy, subclasses 491.1 through 492.3 for irradiating object or material and the ion or electron beam irradiation, per se.

257,　Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for detail structure of active solid-state devices.

324,　Electricity: Measuring and Testing, appropriate subclasses for measuring and testing of electrical devices, in general, particularly subclasses 210 through 212 for magnetic information storage element testing and subclasses 762.01 through 762.1 for testing of a semiconductor device.

326,　Electronic Digital Logic Circuitry, appropriate subclasses for the use of digital components in various types of electronic digital logic circuitries; particularly subclass 10 for the redundancy of circuit components or devices; subclasses 37 through 39, 41, and 47 for the use of programmable devices and their layout interconnections; subclass 38 for the details of setting or programming of interconnections in multifunctional or programmable digital logic circuitry; and subclasses 41 and 47 for significant layout or layout interconnections.

327,　Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for the use of electrical components in various types of active electrical nonlinear circuits or devices.

340,　Communications: Electrical, subclass 14.3 for the use of programmable devices in selective communication.

345,　Computer Graphics Processing and Selective Visual Display Systems, appropriate subclasses for creation and manipulation of graphical objects.

361,　Electricity: Electrical Systems and Devices, subclasses 760 through 783 for the connections of electrical components on a printed circuit board.

430, Radiation Imagery Chemistry: Process, Composition, or Product Thereof, subclass 5 for radiation masks used in radiation imaging of semiconductor devices.

438, Semiconductor Device Manufacturing: Process, appropriate subclasses for the process of manufacturing semiconductor devices.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 121 for computer-controlled semiconductor fabrication.

702, Data Processing: Measuring, Calibrating, or Testing, appropriate subclasses for data processing testing, in general.

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 14 through 16 for circuit and logic simulation.

706, Data Processing: Artificial Intelligence, appropriate subclasses for data processing utilizing knowledge base, rule base, and neural networks.

708, Electrical Computers: Arithmetic Processing and Calculating, appropriate subclasses for arithmetic processing and calculating computer.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses for reliability and availability, particularly subclasses 25 through 46 for fault locating; subclass 30 for scan path testing; and subclasses 724 through 745 for testing and detecting error/fault in one or more circuit components.

SUBCLASSES

30 NANOTECHNOLOGY RELATED INTEGRATED CIRCUIT DESIGN:
This subclass is indented under the class definition. Subject matter comprising means or steps for computer aided design related to the representation, modeling, or design of integrated circuits involving nanotechnology.

50 DESIGN OF SEMICONDUCTOR MASK OR RETICLE:
This subclass is indented under the class definition. Subject matter comprising means or steps for using computer-based tools to aid in planning or devising a template of a circuit pattern to be used for transferring onto a semiconductor wafer.

51 Analysis and verification (process flow, inspection):
This subclass is indented under subclass 50. Subject matter comprising means or steps for analyzing or verifying that a mask or pattern layout conforms to manufacturing-specific design rules or processes.

52 Defect (including design rule checking):
This subclass is indented under subclass 51. Subject matter comprising means or steps for analyzing or verifying mask or pattern layout by performing layout versus schematic analysis or design rule checking.

53 Optical proximity correction (including RET):
This subclass is indented under subclass 51. Subject matter comprises means or steps for compensating for image errors due to diffraction or photoprocess effects.

(1) Note. Examples of optical proximity correction of this subclass type include adding serifs, hammerheads, etc., to the mask pattern or layout pattern so as to overcome optical proximity effects when fabricating the circuit at a higher resolution than normally handled by the lithographic tools.

54 Manufacturing optimizations:
This subclass is indented under subclass 50. Subject matter comprising means or steps for improving physical circuit design representations specifically for fabrication or manufacture (i.e., design for manufacture (DFM)) including lithography-based design improvements.

55 Layout generation (polygon, pattern feature):
This subclass is indented under subclass 50. Subject matter comprising means or steps for generating a mask or pattern layout of the circuit design for fabrication or manufacturing process.

56 Yield:
This subclass is indented under subclass 50. Subject matter comprising means or steps for predicting yield for the circuit design, such as

using aerial image simulation or process specific simulation.

100   INTEGRATED CIRCUIT DESIGN PROCESSING:
This subclass is indented under the class definition. Subject matter comprising means or steps for using computer-based tools to aid in logical and physical design and layout analysis.

101   Logic design processing:
This subclass is indented under subclass 100. Subject matter comprising means or steps wherein a system, functional, or architectural level design representation is analyzed or evaluated, generally in terms of inputs, outputs, and stimuli, in a manner which allows for the design representation to be operated on at various levels by design tools.

     (1)   Note. Subject matter of this subclass type generates design representations (such as High Definition Language (HDL) or Register Transfer Logic (RTL) level representations) that may be analyzed in greater detail, perform other logical behavioral analyses, such as netlist processing (functional and interconnection representations), synthesis, simulations, translations, and verifications.

     (2)   Note. Subject matter of this subclass type usually consists of higher level description representations and may include higher level languages, such as VHDL, C language, graphical representations, and utilization of libraries of behavioral descriptions.

102   Design entry:
This subclass is indented under subclass 101. Subject manner comprising means and steps for generating, analyzing, editing, revising, or modifying a high hardware description language, schematic, or other circuit design representation at various levels of abstraction for use by an electronic design automation (EDA) tool.

103   Translation (logic-to-logic, logic-to-netlist, netlist processing):
This subclass is indented under subclass 101. Subject manner comprising means and steps for converting an original circuit design representation to a target circuit design representation which performs the same function as the original, e.g., netlist creation (a representation of elements and their connections) or a conversion between different programming languages used for circuit representations.

104   Logic circuit synthesis (mapping logic):
This subclass is indented under subclass 101. Subject matter comprising means or steps for determining actual circuit elements and their arrangements which provide desired logical operations.

     (1)   Note. Subject matter may comprise means and steps for implementing a logic or high level circuit design in which a netlist representation of a circuit design is converted into a representation of a target circuit design or a target circuit product or a product family.

     (2)   Note. Subject matter of this subclass type is sometimes called "technology mapping."

105   With partitioning:
This subclass is indented under subclass 104. Subject manner including means or steps for dividing a circuit design into subsections.

106   Design verification (functional simulation, model checking):
This subclass is indented under subclass 101. Subject manner comprising means or steps for checking, evaluating, or verifying functionality or logic of a circuit design.

107   Equivalence checking:
This subclass is indented under subclass 106. Subject manner comprising means or steps for comparing design representations to design requirements or preconditions.

108   Timing verification (timing analysis):
This subclass is indented under subclass 106. Subject manner comprising means or steps for performing timing analysis or timing verification on the logic or high level circuit design.

     (1)   Note. Steps may include verification and analysis of the logical, sequential flow of signals or switching operations of circuit element representations using meth-

ods such as finite state machines (FSMs), binary decision diagrams (BDDs), or other methods which may verify or analyze the logical state of signals or circuit elements.

109 Power estimation:
This subclass is indented under subclass 106. Subject manner comprising means or steps for analyzing, evaluating, or estimating power consumption of a circuit design.

110 Physical design processing:
This subclass is indented under subclass 100. Subject matter comprising means or steps for creating an actual, physical, geometrical design of an integrated circuit.

(1) Note. Steps may include the entry or creation of floorplans of circuit elements, placing and routing between circuit elements, optimization, and verifications techniques which prepare a circuit design prior to mask making and integrated circuit manufacture.

(2) Note. This subclass is intended to include circuit design representations that include the physical nature of integrated circuit elements such as transistors, resistors, capacitors, diodes, wires, or signal traces, interactions of circuit elements with respect to each other, or the physical medium in which they will be formed.

111 Verification:
This subclass is indented under subclass 110. Subject matter comprising means or steps for checking and confirming the circuit component layout or routing for consistency or correctness.

112 Defect analysis:
This subclass is indented under subclass 111. Subject matter wherein the design verification comprises means or steps for determining layout or routing compliance with specifications, design rule requirements, etc.

(1) Note. Subject matter of this subclass type includes, for example, Layout Versus Schematic (LVS) and Design Rule Checking (DRC) techniques.

113 Timing analysis:
This subclass is indented under subclass 111. Subject matter wherein the design verification is confirmed based on timing constraints such as delay or slack of the circuit components with respect to layout/routing, critical paths, static timing analysis, etc.

114 Buffer or repeater insertion:
This subclass is indented under subclass 113. Subject matter wherein the findings of timing analysis are addressed by the insertion of circuit components such as buffers, repeaters, inverters, scan chains, etc.

115 Noise (e.g., crosstalk, electromigration, etc.):
This subclass is indented under subclass 111. Subject matter wherein the design verification involves detecting or evaluating possible sources of undesired signal components, e.g., parasitic parameters, victim/aggressor nets, width/length characteristics, etc.

116 Mapping circuit design to programmable logic devices (PLDs):
This subclass is indented under subclass 110. Subject matter comprising means or steps for automatically transforming or converting a circuit design into a programmable implementation.

(1) Note. Programmable logic devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

(2) Note. Transformed or converted circuit designs of this subclass type include, for example, specifications, high-level descriptions, netlists, Boolean expressions, etc. Programmable implementations of this subclass type include, for example, configurable logic blocks (CLBs), look-up tables (LUTs), registers, etc.

117 Configuring PLDs (including data file, bitstream generation, etc.):
This subclass is indented under subclass 116. Subject matter wherein a file or bitstream is generated from the mapped PLD which defines how the circuit components on the PLD are arranged, placed, routed, etc.

118   Floorplanning:
This subclass is indented under subclass 110. Subject matter comprising means or steps for placing circuit block units or cells on a layout area of an LSI or PCB.

     (1)   Note. Floorplanning of this subclass type occurs at the initial designing stage.

119   Placement or layout:
This subclass is indented under subclass 118. Subject matter comprising means or steps for refining the floorplan, i.e., refining the position assignment or the size or the shape of the circuit block units or cells.

120   Power distribution:
This subclass is indented under subclass 119. The subject matter comprising means or steps for refining the position assignment, size, or shape of circuit block units, cells, or clock tree structures (components) for the purpose of gaining a desired placement of components and the respective power distribution.

121   For PLDs:
This subclass is indented under subclass 119. The subject matter comprising means or steps for refining the position assignment, size, or shape of circuit block units, cells, or (programmable) logic elements on a programmable logic device, such as FGPAs, ASICs, etc.

     (1)   Note. Programmable Logic Devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

122   Constraint-based:
This subclass is indented under 119. Subject matter wherein the arrangement of circuit block units or circuit components must satisfy one or more positional assignment restraints.

123   Iteration:
This subclass is indented under subclass 119. Subject matter comprising means or steps for repeatedly adjusting and evaluating the position assignment, size, or shape of the circuit block units or cells to improve the efficiency of the floorplan.

124   With partitioning:
This subclass is indented under subclass 119. Subject matter comprising means or steps for dividing the circuit design into a set of smaller sub-circuits.

125   With partitioning:
This subclass is indented under subclass 118. Subject matter comprising means or steps for dividing the circuit design into a set of smaller sub-circuits.

126   Routing:
This subclass is indented under subclass 110. Subject matter comprising means or steps for determining interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins).

127   Power (voltage islands):
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the interconnection paths with respect to power to or between circuit blocks, cells, or components of an integrated circuit.

128   PLDs:
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the interconnection of paths to or between logic elements of a programmable logic device (PLD), including the wiring within the logic elements, and the wiring, or switching techniques used for the connections between elements.

     (1)   Note. Programmable Logic Devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

129   Global:
This subclass is indented under subclass 126. Subject matter comprising means or steps for evaluating or determining the shortest interconnection paths or minimizing the number of channels required for placing the conductor paths between nets.

130   Detailed:
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the wiring route within a specified circuit region.

  (1)   Note. A detailed router searches and finds the actual geometric layout of a specific circuit region and considers only one region at a time as opposed to global router which considers the entire circuit regions of the layout.

  (2)   Note. Detailed routing includes channel routing and switch box routing.

131   With partitioning:
This subclass is indented under subclass 126. Subject matter comprising means or steps wherein determining the interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins) involves dividing or sectioning the layout.

132   Optimization:
This subclass is indented under subclass 100. Subject matter comprising means or steps for improving a circuit design by improving the logic design representation through the use of an algorithm or other compaction or minimization method, or by improving the physical circuit design by specific constraints or criteria.

133   For power:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to power to or between circuit elements.

134   For timing:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to timing to or between circuit elements.

135   For area:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to the layout of design elements on a circuit design space.

136   Testing or evaluating:
This subclass is indented under subclass 100. Subject matter comprising means or steps for determining, i.e., testing or evaluating, the performance of the circuit or component design.

137   PCB, MCM design:
This subclass is indented under subclass 100. Subject matter comprising means or steps for sketching, outlining, or defining the layout or routing of circuit components on a printed circuit board (PCB), printed wiring board (PWB), or multi-chip module (MCM).

138   System-on-chip design:
This subclass is indented under subclass 100. Subject matter comprising means or steps for sketching, outlining, or defining the layout or routing of circuit components contained on a single chip.

139   Layout editor (with ECO, reuse, GUI):
This subclass is indented under subclass 100. Subject matter comprising means or steps for interactively using a workstation or graphical user interface (GUI) to sketch, outline, or define the layout or routing of circuit components.

FOREIGN ART COLLECTIONS

The definitions below correspond to abolished subclasses from which these collections were formed. See the Foreign Art Collection schedule of this class for specific correspondences. [Note: The titles and definitions for indented art collections include all the details of the one(s) that are hierarchically superior.]

FOR 100   CIRCUIT DESIGN:
Foreign art collection including subject matter comprising means or steps for sketching or outlining of layout of circuit components.

FOR 101   Optimization (e.g., redundancy, compaction):
Foreign art collection including subject matter comprising means or steps for improving the layout of the designed circuit components as far as possible.

  (1)   Note. Examples of the circuit design improvements are global redundancy or compaction of the designed circuit lay-

out such that preserving the integrity of the original circuit design in compliance with design rule requirements.

FOR 102 Translation (e.g., conversion, equivalence):
Foreign art collection including subject matter comprising means or steps for converting an original circuit design data to a target circuit design data having different circuit components while performing the same function as the original circuit design by utilizing a rule group for the conversion.

(1)   Note. Rule group, design rule, or design specification have substantially the same meaning. They refer to a set of regulations which define the acceptable dimensions and electrical characteristics achievable in a fabrication process.

FOR 103 Testing or evaluating:
Foreign art collection including subject matter comprising means or steps for determining (i.e., evaluating) the performance of the designed circuit components.

FOR 104 Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width):
Foreign art collection including subject matter comprising means or steps for checking and confirming the circuit component s layout for consistency of the functional and logical correctness.

FOR 105 Timing analysis (e.g., delay time, path delay, latch timing):
Foreign art collection including subject matter wherein the design verification is confirmed based on timing constraints such as delay or latch timing of the circuit components.

FOR 106 Partitioning (e.g., function block, ordering constraint):
Foreign art collection including subject matter comprising means or steps for dividing the circuit design into a set of smaller subcircuits arranged in a logical hierarchical structure.

FOR 107 Floorplanning:
Foreign art collection including subject matter comprising means or steps for enabling exact judgment of accommodation feasibility of using circuit block units or cells on a layout area of an LSI or PCB at the initial designing stage.

FOR 108 Detailed placement (i.e., iterative improvement):
Foreign art collection including subject matter comprising means or steps for refining the position assignment, the size or the shape of the circuit block units or cells, and evaluating repeatedly the position assignment of the block units or cells until all the cells are replaced as efficiently as possible in a refined portion of the floor planned layout of a PCB or an LSI.

FOR 109 Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance):
Foreign art collection including subject matter wherein the arrangement of circuit block units or circuit components must satisfy one or more positional assignment restraints.

FOR 110 Layout editor (e.g., updating):
Foreign art collection including subject matter comprising means or steps for revising or modifying the circuit layout interactively by utilizing graphical representations such as icons or menus.

FOR 111 Routing (e.g., routing map, netlisting):
Foreign art collection including subject matter comprising means or steps for determining the interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins).

(1)   Note. Connection of terminals or nets at the periphery of a block to the terminals of another block is called a netlist.

(2)   Note. Netlisting or process of generating a netlist is included in this subclass.

FOR 112 Global routing (e.g., shortest path, dead space, or duplicate trace elimination):
Foreign art collection including subject matter comprising means or steps for evaluating or determining the shortest interconnection paths or minimizing the number of channels

required for placing the conductor paths between nets.

(1)   Note. In global routing, the wiring path capacities in a path net or between plural path routing regions and their relationships are usually modeled as graph or trees.

(2)   Note. Procedures for determining the shortest paths may include, for example, Maze routing algorithm, Lee's algorithm, Soukup's algorithm, Hadlock's algorithm, or Steiner tree-based algorithm.

FOR 113   Detailed routing (e.g., channel routing, switch box routing):
Foreign art collections including subject matter comprising means or steps for determining the wiring route within a specified circuit region.

(1)   Note. A detailed router searches and finds the actual geometric layout of a specific circuit region and considers only one region at a time as opposed to global router which considers the entire circuit regions of the layout.

(2)   Note. Detailed routing includes channel routing and switch box routing.

FOR 114   PCB wiring:
Foreign art collection including subject matter including the routing paths or wiring of circuit components on a printed circuit board.

FOR 115   PLA, PLD, FPGA or MCM:
Foreign art collection including subject matter wherein the circuit components are programmable logic arrays or devices, field programmable gate arrays, or multichip modules.

FOR 116   Programmable integrated circuit (e.g., basic cell, standard cell, macrocell):
Foreign art collection including subject matter wherein the designed circuit utilizes a high-level circuit element such as an arithmetic or logical component selectively operable (i.e., programmable component) to perform a given or required specific combinational function.

FOR 117   Logical circuit synthesizer:
Foreign art collection including subject matter comprising means or steps for automatically transforming a high-level design (e.g., functional specification or functional-level logic such as Boolean expression, truth table, or standard macro logic) into its hardware implementation.

FOR 118   DESIGN OF SEMICONDUCTOR MASK:
Foreign art collection including subject matter comprising means or steps for planning or devising a template used for etching circuit pattern on semiconductor wafers.

FOR 119   Mesh generation:
Foreign art collection including subject matter comprising means or steps for determining or approximating the surface contour of the mask by mathematical model or algorithm such as numerical analysis.

(1)   Note. The shape or boundary of the mask is divided or segmented into rectangular, triangular, or polygon grids for approximation, for example, by differential equations algorithm.

FOR 120   Pattern exposure:
Foreign art collection including subject matter including means or steps for tracing or drawing an electronic pattern on a semiconductor wafer or mask with particle beam.

(1)   Note. Examples of particle beams are ion beams, electron beams, or e-beams.

FOR 489   Circuit DESIGN AND ANALYSIS (364/ 489):
Foreign art collection for subject matter wherein the components are electrical components interconnected into functional configurations.

FOR 490   Integrated (364/490):
Foreign art collection for subject matter wherein the circuits are a combination of interconnected circuit elements inseparably associated on or within a continuous substrate.

FOR 491 **Layout (364/491):**
Foreign art collection for subject matter comprising means or steps for designing and analyzing topological arrangement of conductors and components in an integrated circuit.

END